UCC2742x-EP Dual 4-A High-Speed Low-Side MOSFET Driver With Enable

1 Features

- Industry-Standard Pinout
- Enable Functions for Each Driver
- High Current-Drive Capability of ±4 A
- Unique Bipolar and CMOS True-Drive Output Stage Provides High Current at MOSFET Miller Thresholds
- TTL-/CMOS-Compatible Inputs Independent of Supply Voltage
- 20-ns Typical Rise and 15-ns Typical Fall Times With 1.8-nF Load
- Typical Propagation Delay Times of 25 ns With Input Falling and 35 ns With Input Rising
- 4.5-V to 15-V Supply Voltage
- Dual Outputs can be Paralleled for Higher Drive Current
- Available in Thermally-Enhanced MSOP PowerPAD™ Package With 4.7°C/W $R_{\theta JC}$
- Supports Defense, Aerospace, and Medical Applications
  - Controlled Baseline
  - One Assembly/Test Site
  - One Fabrication Site
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability

2 Applications

- Switch-Mode Power Supplies
- DC/DC Converters
- Motor Controllers
- Line Drivers
- Class-D Switching Amplifiers

3 Description

The UCC27423 and UCC27424 high-speed MOSFET drivers can deliver large peak currents into capacitive loads. Two standard logic options are offered – dual inverting and dual noninverting drivers. The UCC27424 thermally-enhanced 8-pin PowerPAD™ MSOP package (DGN) drastically lowers the thermal resistance to improve long-term reliability. The UCC27423 is offered in a standard SOIC-8 (D) package.

Using a design that inherently minimizes shoot-through current, this driver delivers 4 A of current where it is needed most – at the Miller plateau region during the MOSFET switching transition. A unique bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing and sinking at low supply voltages.

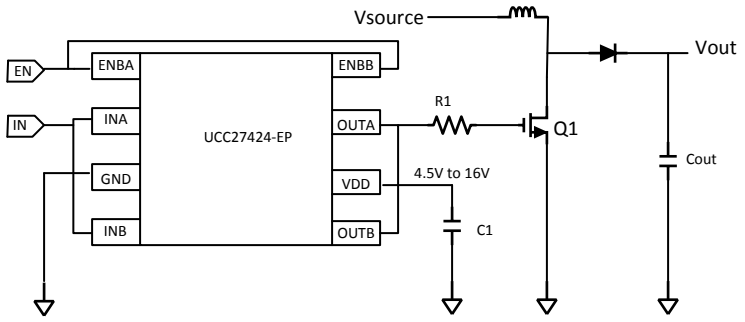
The UCC27423 and UCC27424 provide enable (ENB) functions to better control the operation of the driver applications. ENBA and ENBB are implemented on pins 1 and 8, which previously were left unused in the industry-standard pinout. ENBA and ENBB are pulled up internally to V_{DD} for active-high logic and can be left open for standard operation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27423-EP	D (8)	3.91 mm × 4.90 mm
UCC27424-EP	DGN (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2012) to Revision C — **Page**

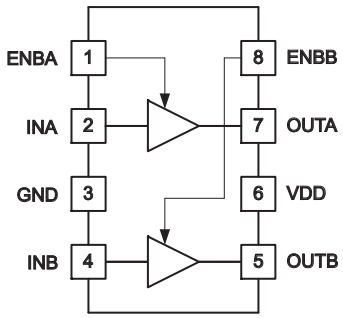
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (November, 2009) to Revision B — **Page**

- Changed minimum supply voltage from 4-V to 4.5-V in *Features* section ... 1
- Changed Figure 11, Rise Time vs Supply Voltage ... 8
- Changed Figure 12 Fall Time vs Supply Voltage ... 8
- Changed first paragraph of *Operational Waveforms and Circuit Layout* section ... 13
- Changed Figure 25, Current Sinking ... 16
- Changed Figure 26, Current Sourcing ... 16

5 Pin Configuration and Functions

D or DGN Package
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ENBA	1	I	Enable for driver A with logic-compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is pulled up internally to V_{DD} with a 100-kΩ resistor for active-high operation. When the device is disabled, the output state is low, regardless of the input state.
ENBB	8	I	Enable for driver B with logic-compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is pulled up internally to VDD with a 100-kΩ resistor for active-high operation. The output state when the device is disabled is low, regardless of the input state.
GND	3	—	Common ground. This ground should be connected very closely to the source of the power MOSFET that the driver is driving.
INA	2	I	Input A. Input signal of the A driver, which has logic-compatible threshold and hysteresis. If not used, this input should be tied to either VDD or GND. Do not leave floating.
INB	4	I	Input B. Input signal of the A driver, which has logic-compatible threshold and hysteresis. If not used, this input should be tied to either VDD or GND. Do not leave floating.
OUTA	7	O	Driver output A. The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
OUTB	5	O	Driver output B. The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
VDD	6	I	Supply. Supply voltage and the power input connection for this device.

6 Specifications

6.1 Absolute Maximum Ratings (1) (2)

over operating free-air temperature range (unless otherwise noted)

				MN	MAX	UNIT
V_{DD}	Supply voltage			–0.3	16	V
	Output current	OUTA, OUTB	DC, I_{OUT_DC}		0.2	A
			Pulsed (0.5 μs), I_{OUT_PULSED}		4.5	
V_{IN}	Input voltage	INA, INB		–5	6 or V_{DD} + 0.3 (3)	V
	Enable voltage	ENBA, ENBB		–0.3	6 or V_{DD} + 0.3 (3)	V
	Power dissipation at T_A = 25°C	D package			650	mW
		DGN package			3	W
T_J	Junction operating temperature			–55	150	°C
	Lead temperature (soldering, 10 s)				300	°C
T_{stg}	Storage temperature			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.
(3) Whichever is larger

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_J	Operating junction temperature	–55	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC27423-EP	UCC27424-EP	UNIT
		D	DGN	
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.4		°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.8		
$R_{\theta JB}$	Junction-to-board thermal resistance	56.6		
ψ_{JT}	Junction-to-top characterization parameter	10.9		
ψ_{JB}	Junction-to-board characterization parameter	56.1		

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Power Dissipation Ratings

PACKAGE	SUFFIX	$R_{\theta JC}$ (°C/W)	$R_{\theta JA}$ (°C/W)	POWER RATING (mW) T_A = 70°C	DERATING FACTOR ABOVE 70°C (mW/°C)
MSOP-8 PowerPAD(1)	DGN	4.7	50 to 59	1370(2)	17.1(2)
SOIC 8	D	42	84 to 160	344 to 655(3)(4)	6.25 to 11.9(3)(4)

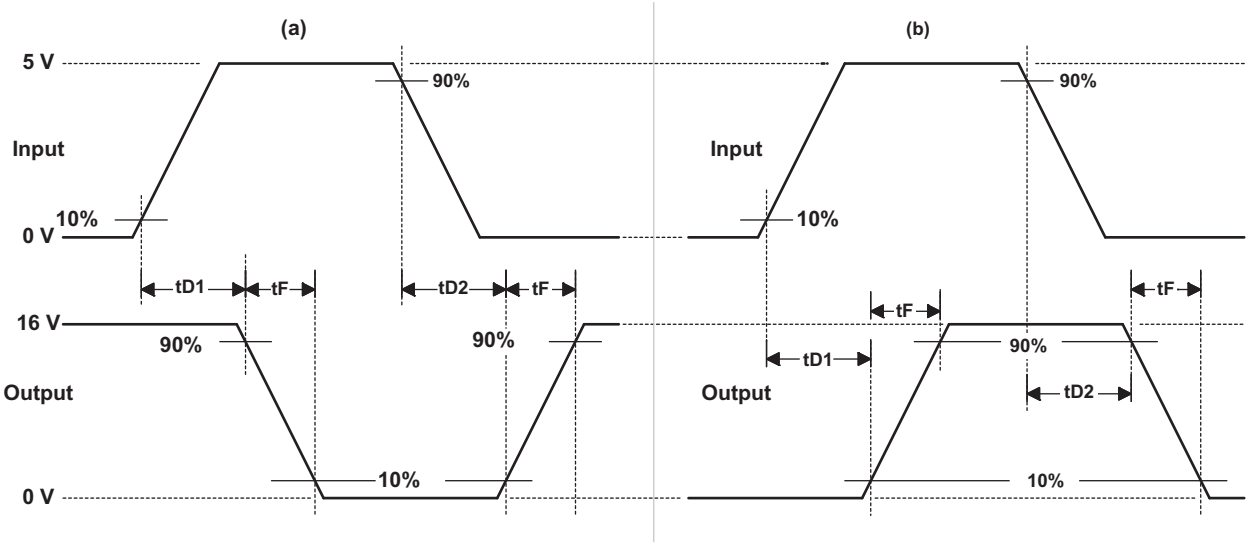
(1) The PowerPAD package is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.
(2) 150°C operating junction temperature is used for power-rating calculations.
(3) The range of values indicates the effect of PCB. These values are intended to give the system designer an indication of the best- and worst-case conditions. In general, the system designer should attempt to use larger traces on the PCB where possible, in order to spread the heat away from the device more effectively. For information on the PowerPAD package, refer to technical brief, *PowerPad™ Thermally-Enhanced Package*, SLMA002, and application brief, *PowerPad™ Made Easy*, SLMA004.
(4) 125°C operating junction temperature is used for power-rating calculation.

6.6 Electrical Characteristics

V_{DD} = 4.5 V to 15 V, T_A = –55°C to 125°C, T_A = T_J (unless otherwise noted)

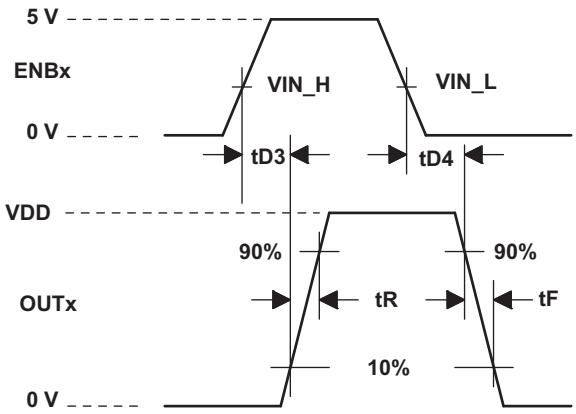
PARAMETER		TEST CONDITIONS		UCC27423			UCC27424			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT (INA, INB)										
V_{IN_H}	Logic 1 input threshold			2			2			V
V_{IN_L}	Logic 0 input threshold					1			1	V
	Input current	0 V ≤ V_{IN} ≤ V_{DD}		–10	0	10	–10	0	10	µA
OUTPUT (OUTA, OUTB)										
	Output current	V_{DD} = 14 V(1) (2)			4			4		A
V_{OH}	High-level output voltage	V_{OH} = V_{DD} – V_{OUT}, I_{OUT} = –10 mA			330	450		330	450	mV
V_{OL}	Low-level output level	I_{OUT} = 10 mA			22	40		22	40	mV
	Output resistance high	I_{OUT} = –10 mA, V_{DD} = 14 V(3)	T_A = 25°C	25	30	35	25	30	35	Ω
			T_A = full range	14		45	18		45	
	Output resistance low	I_{OUT} = –10 mA, V_{DD} = 14 V(3)	T_A = 25°C	1.9	2.2	2.5	1.9	2.2	2.5	Ω
			T_A = full range	0.95		4	1.2		4	
	Latch-up protection(1)			500			500			mA
SWITCHING TIME										
t_R	Rise time (OUTA, OUTB)	C_{LOAD} = 1.8 nF(1)			20	40		20	40	ns
t_F	Fall time (OUTA, OUTB)	C_{LOAD} = 1.8 nF(1)			15	40		15	40	ns
t_{D1}	Delay, IN rising (IN to OUT)	C_{LOAD} = 1.8 nF(1)			35	55		35	50	ns
t_{D2}	Delay, IN falling (IN to OUT)	C_{LOAD} = 1.8 nF(1)			25	60		25	45	ns
ENABLE (ENBA, ENBB)										
V_{IN_H}	High-level input voltage	Low-to-high transition		1.7	2.4	3.1	1.7	2.4	2.9	V
V_{IN_L}	Low-level input voltage	High-to-low transition		1.1	1.8	2.3	1.1	1.8	2.2	V
	Hysteresis			0.13	0.55	1.1	.10	0.55	0.9	V
R_{ENBL}	Enable impedance	V_{DD} = 14 V, ENBL = GND		75	100	160	75	100	140	kΩ
t_{D3}	Propagation delay time(4)	C_{LOAD} = 1.8 nF(1)			30	60		30	60	ns
t_{D4}	Propagation delay time(4)	C_{LOAD} = 1.8 nF(1)			100	150		100	150	ns
OVERALL										
I_{DD}	Static operating current, V_{DD} = 15 V, ENBA = ENBB = 15 V	INA = 0 V	INB = 0 V		900	1350		300	450	µA
			INB = High		750	1100		750	1100	
		INA = HIGH	INB = 0 V		750	1100		750	1100	
			INB = High		600	900		1200	1800	
	Disabled, V_{DD} = 15 V, ENBA = ENBB = 0 V	INA = 0 V	INB = 0 V		300	450		300	450	
			INA = High		450	700		450	700	
		INA = HIGH	INB = 0 V		450	700		450	700	
			INB = High		600	900		600	900	

(1) Specified by design. Not tested in production.
(2) The pullup/pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The pulsed output current rating is the combined current from the bipolar and MOSFET transistors.
(3) The pullup/pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.
(4) See Figure 2.



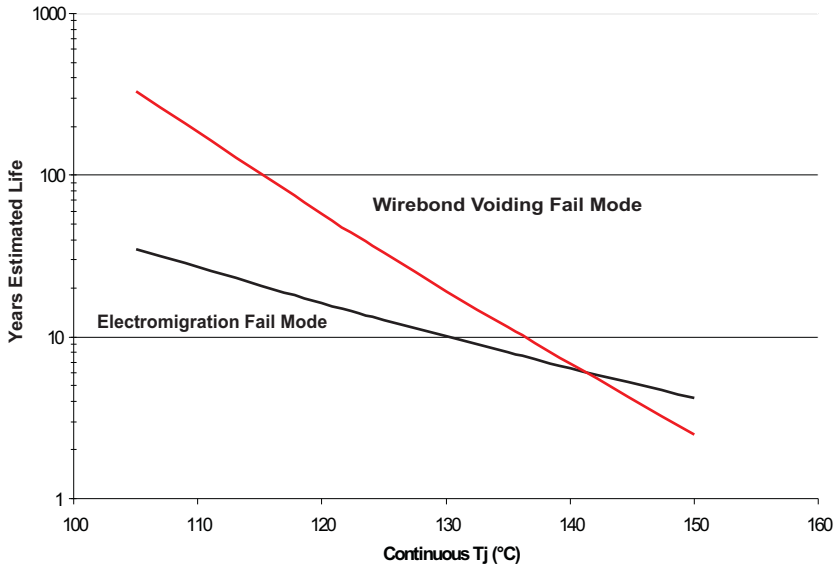
A. The 10% and 90% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 1. Switching Waveforms for (a) Inverting Driver and (b) Noninverting Driver



A. The 10% and 90% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 2. Switching Waveform for Enable to Output



A. See data sheet for absolute maximum and minimum recommended operating conditions.

B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

C. Enhanced plastic product disclaimer applies

Figure 3. UCC27424MDGNREP Operating Life Derating Chart

6.7 Typical Characteristics

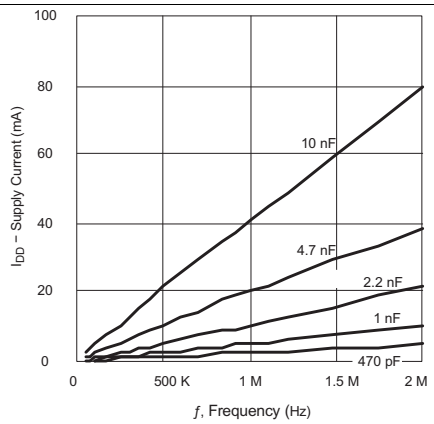


Figure 4. Supply Current vs Frequency (V_{DD} = 4.5 V)

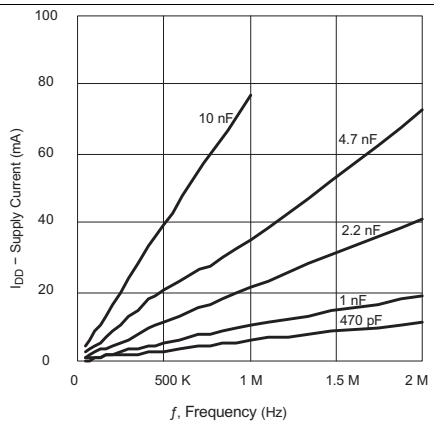


Figure 5. Supply Current vs Frequency (V_{DD} = 8 V)

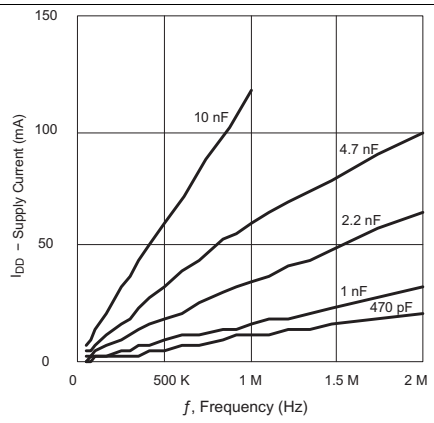


Figure 6. Supply Current vs Frequency (V_{DD} = 12 V)

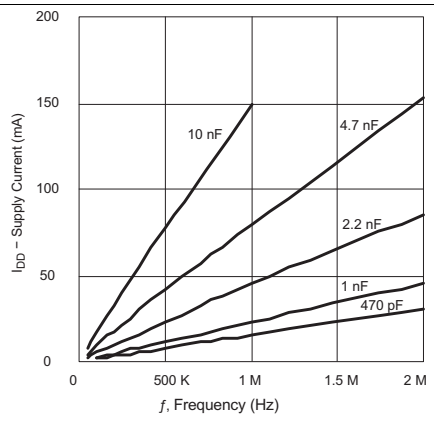


Figure 7. Supply Current vs Frequency (V_{DD} = 15 V)

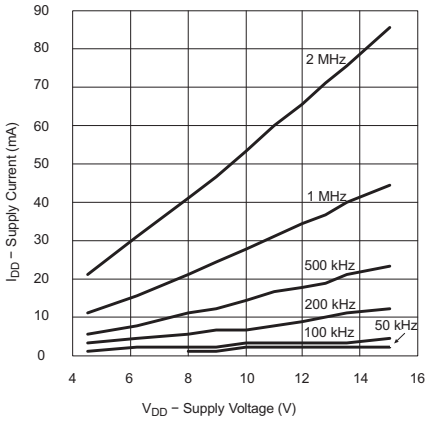


Figure 8. Supply Current vs Supply Voltage (C_{LOAD} = 2.2 nF)

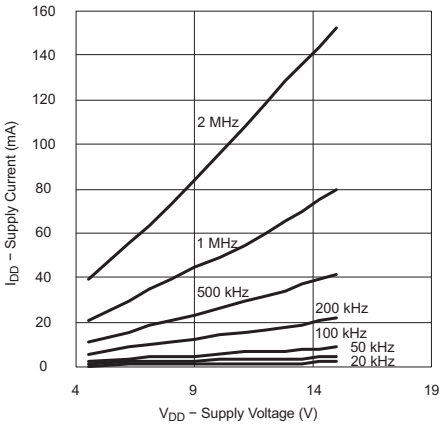


Figure 9. Supply Current vs Supply Voltage (C_{LOAD} = 4.7 nF)

Typical Characteristics (continued)

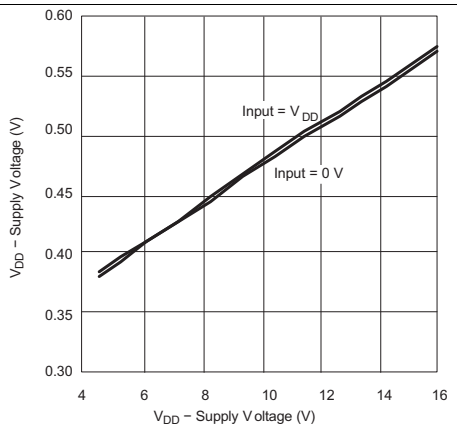


Figure 10. Supply Current vs Supply Voltage

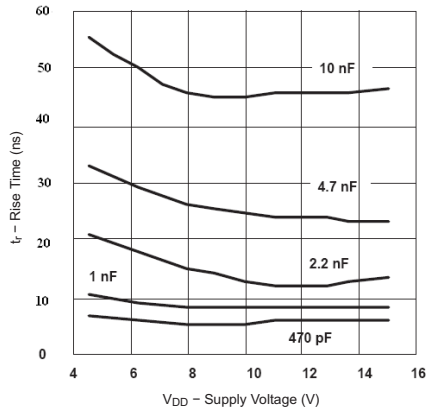


Figure 11. Rise Time vs Supply Voltage

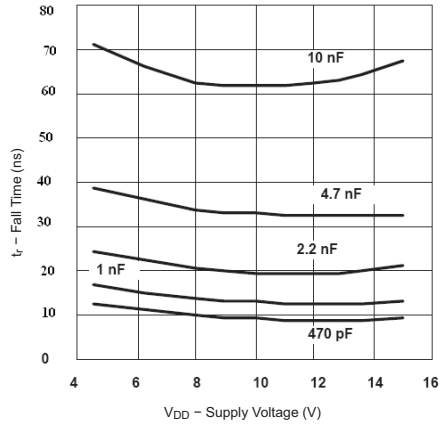


Figure 12. Fall Time vs Supply Voltage

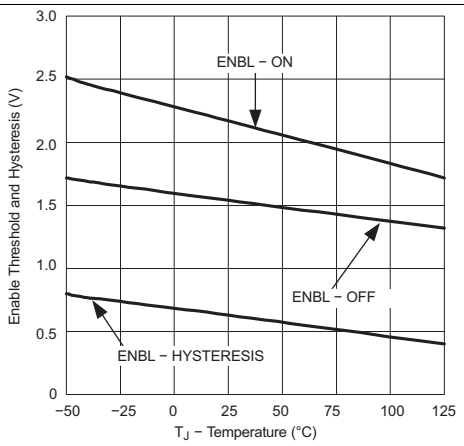


Figure 13. Enable Threshold and Hysteresis vs Temperature

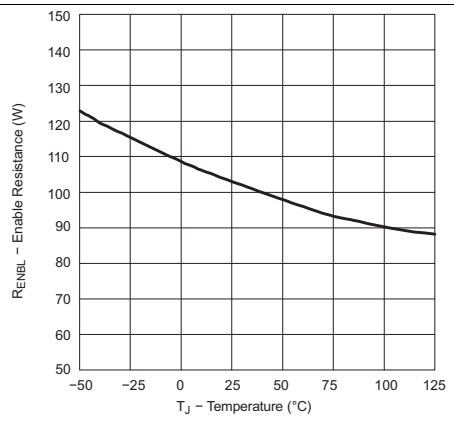


Figure 14. Enable Resistance vs Temperature

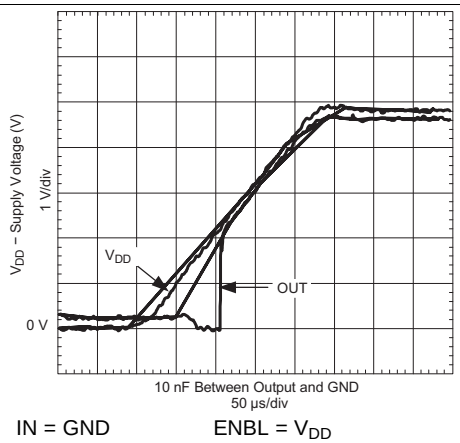
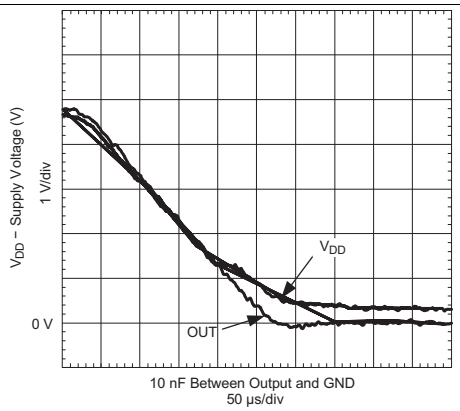


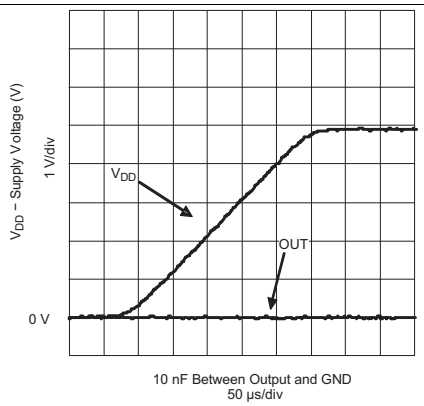
Figure 15. Output Behavior vs Supply Voltage (Inverting)

Typical Characteristics (continued)



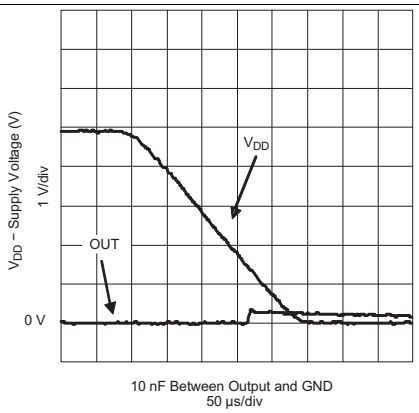
IN = GND ENBL = V_{DD}

Figure 16. Output Behavior vs Supply Voltage (Inverting)



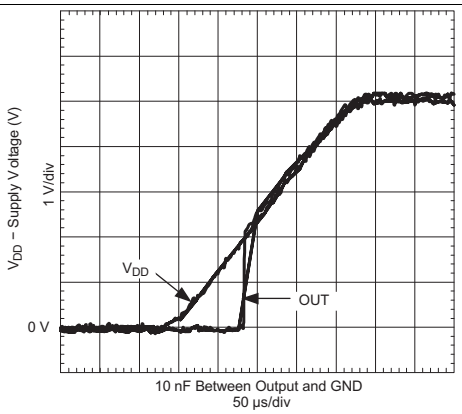
IN = V_{DD} ENBL = V_{DD}

Figure 17. Output Behavior vs V_{DD} (Inverting)



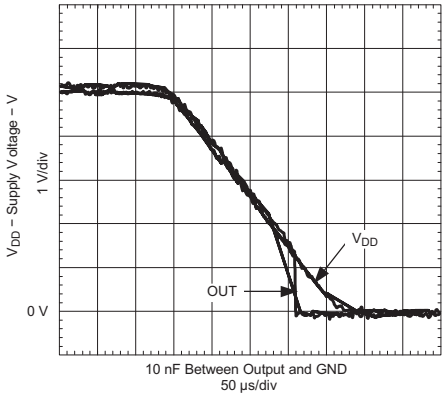
IN = V_{DD} ENBL = V_{DD}

Figure 18. Output Behavior vs V_{DD} (Inverting)



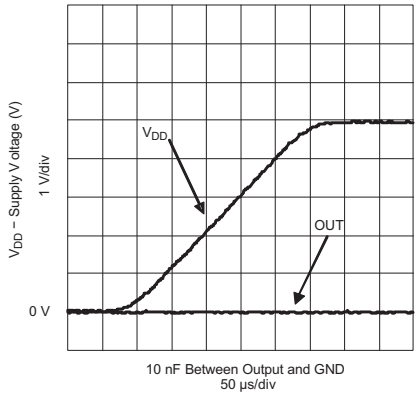
IN = V_{DD} ENBL = V_{DD}

Figure 19. Output Behavior vs V_{DD} (Noninverting)



IN = V_{DD} ENBL = V_{DD}

Figure 20. Output Behavior vs V_{DD} (Noninverting)



IN = GND ENBL = V_{DD}

Figure 21. Output Behavior vs V_{DD} (Noninverting)

Typical Characteristics (continued)

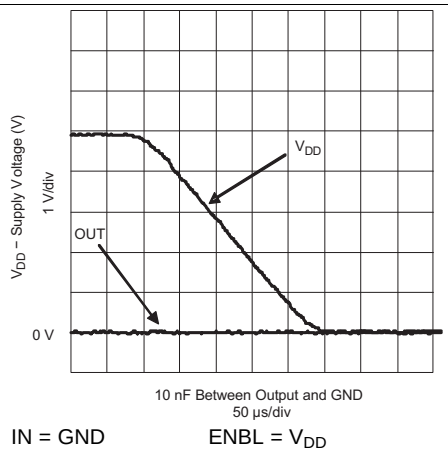


Figure 22. Output Behavior vs V_{DD} (Noninverting)

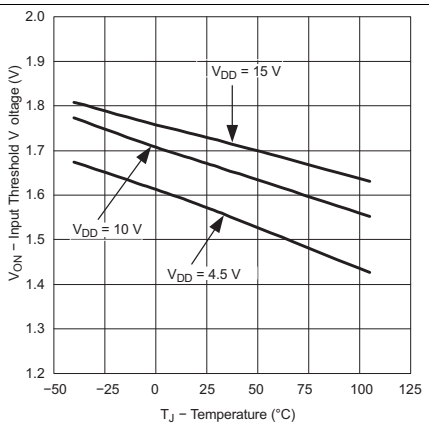


Figure 23. Input Threshold vs Temperature

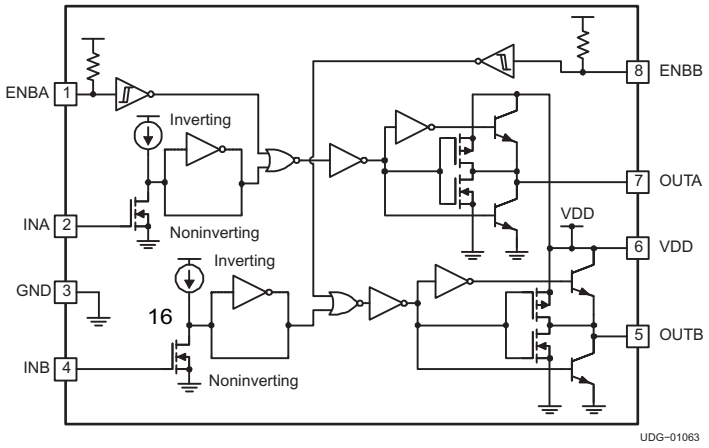
7 Detailed Description

7.1 Overview

High-frequency power supplies often require high-speed, high-current drivers such as the UCC2742x. A leading application of the UCC2742x provides a high-power buffer stage between the pulse-duration modulation (PWM) output of the control IC and the gates of the primary power MOSFET or insulated gate bipolar transistor (IGBT) switching devices. In other cases, the driver IC is used to drive the power-device gates through a drive transformer. Synchronous rectification supplies also have the need to simultaneously drive multiple devices, which can present an extremely-large load to the control circuitry.

Driver ICs are used when it is not feasible to have the primary PWM regulator IC directly drive the switching devices, for one or more reasons. The PWM IC may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases, there may be a desire to minimize the effect of high-frequency switching noise by placing the high-current driver physically close to the load. Also, newer ICs that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are intended to drive only the high-impedance input to drivers such as the UCC2742x. Finally, the control IC may be under thermal stress due to power dissipation, and an external driver can help by moving the heat from the controller to an external package.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Stage

The input thresholds have a 3.3-V logic sensitivity over the full range of V_{DD} voltages. However, they are equally compatible with 0 to V_{DD} signals. The inputs of the UCC2742x are designed to withstand 500-mA reverse current without either damage to the IC or logic upset. The input stage of each driver should be driven by a signal with a short rise or fall time. This condition is satisfied in typical power-supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The input stages to the drivers function as a digital gate, and they are not intended for applications where a slow-changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an effort to slow down (or delay) the signal at the output. If limiting the rise or fall times to the power device is desired, limit the rise or fall times to the power device. Then, the user can add an external resistance between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor also may help remove power dissipation from the device package, as discussed in *Thermal Considerations*.

Feature Description (continued)

7.3.2 Output Stage

Inverting outputs of the UCC27423 are intended to drive external P-channel MOSFETs. Noninverting outputs of the UCC27424 are intended to drive external N-channel MOSFETs.

Each output stage is capable of supplying ±4-A peak current pulses and swings to both VDD and GND. The pullup/ pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very-low impedance to overshoot and undershoot, due to the body diode of the external MOSFET. This means that, in many cases, external Schottky clamp diodes are not required.

The UCC27423 family delivers the 4-A gate drive where it is most needed during the MOSFET switching transition, at the Miller plateau region, providing efficiency gains. A unique bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing at low supply voltages.

7.3.3 Operational Waveforms and Circuit Layout

Sink and source currents of the driver depend on V_{DD} value and the output capacitive load. The larger the V_{DD} value, the higher the current capability. Also, the larger the capacitive load, the higher the current and source capabilities.

See Figure 28 for pulse response.

Trace resistance and inductance, including wires and cables for testing, slow down the rise and fall times of the outputs. Thus, the driver's current capabilities are reduced. See *Layout Guidelines* for more information on how to achieve higher current results.

In a power driver operating at high frequency, it is a significant challenge to get clean waveforms without much overshoot/undershoot and ringing. The low output impedance of these drivers produces waveforms with high di/dt. This tends to induce ringing in the parasitic inductances. See *Layout Guidelines* for more information.

7.3.4 VDD

Although quiescent VDD current is very low, total supply current will be higher, depending on OUTA and OUTB current and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), calculate the average OUT current with Equation 1.

$$I_{OUT} = Q_g \times f \quad (1)$$

where

- f is frequency

For the best high-speed circuit performance, TI recommends two V_{DD} bypass capacitors to prevent noise problems. TI highly recommends the use of surface-mount components. A 0.1-µF ceramic capacitor should be located closest to the VDD-to-ground connection. In addition, a larger capacitor (such as 1 µF) with relatively-low ESR should be connected in parallel, to help deliver the high-current peaks to the load. The parallel combination of capacitors should present a low-impedance characteristic for the expected current levels in the driver application.

7.3.5 Enable

The UCC2742x provides dual-enable inputs for improved control of each driver channel operation. The inputs incorporate logic-compatible thresholds with hysteresis. They are pulled internally up to V_{DD} with a 100-kΩ resistor for active-high operation. When ENBA and ENBB are driven high, the drivers are enabled, and when ENBA and ENBB are low, the drivers are disabled. The default state of the enable pin is to enable the driver, and therefore, can be left open for standard operation. When the drivers are disabled, the output states are low, regardless of the input state. See Table 1 for a truth table of the operation using enable logic.

Enable inputs are compatible with both logic signals and slow-changing analog signals. They can be driven directly or a power-up delay can be programmed with a capacitor between ENBA, ENBB, and AGND. ENBA and ENBB control input A and input B, respectively.

7.4 Device Functional Modes

Table 1. Pin Inputs and Outputs

		INPUTS (VIN_L, VIN_H)		OUTPUTS	
ENBA	ENBB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	X	X	L	L

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

UCC2742x-EP is designed for high-speed and high-operating reliability. UCC2742x family of gate driver is capable of delivering 4 A into capacitive load. Inverting outputs of UCC27423 are intended to drive external P-Channel MOSFETs and noninverting outputs of UCC27424 are intended to drive external N-channel MOSFETs.

8.2 Typical Application

Figure 24 shows typical application of UCC2742x device when used as a gate driver for the power MOSFET in boost converter application.

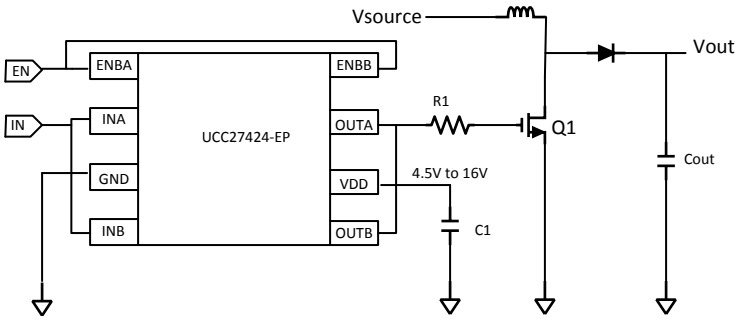


Figure 24. Typical Application Schematic

8.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first in order to make the most appropriate selection. Among these considerations are input-to-output configuration, input threshold type, bias supply voltage, peak source and sink current, availability of independent enable and disable function, propagation delay, power dissipation and package type.

Table 2. Design Parameters

Parameters	Value
Supply voltage	4.5 to 15 V
Output source current	4 A
Output sink current	4 A
Propagation delay	25 ns
Rise time	20 ns
Fall time	15 ns

8.2.2 Detailed Design Procedure

Propagation Delay:

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC2742x-EP device features 25 ns (typical) propagation delay which ensures very little pulse distortion and allows operation at high frequencies.

8.2.2.1 Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC2742x drivers are optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver device. [1]

Two circuits are used to test the current capabilities of the UCC27423 driver. In each case, external circuitry is added to clamp the output near 5 V while the IC is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. Each test showed a transient period where the current peaked up and then settled down to a steady-state value. The noted current measurements are made 200 ns after the input pulse is applied, following the initial transient.

The first circuit in Figure 25 is used to verify the current sink capability when the output of the driver is clamped around 5 V (a typical value of gate-source voltage during the Miller plateau region). The UCC27423 is found to sink 4.5 A at V_{DD} = 15 V and 4.28 A at V_{DD} = 12 V.

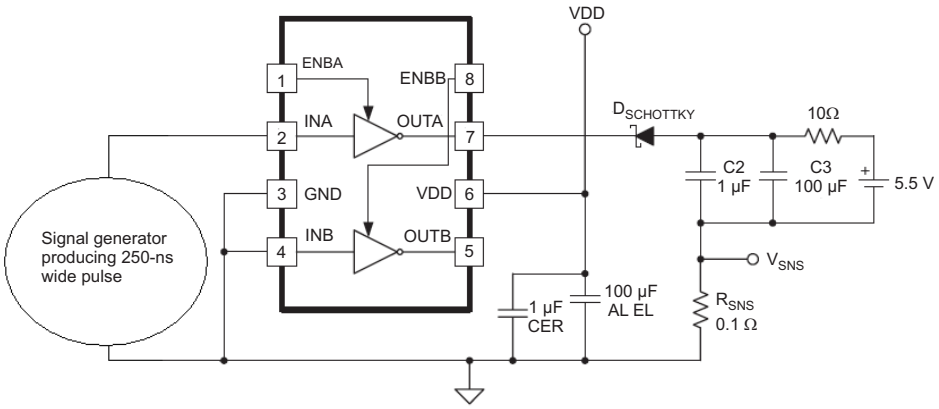


Figure 25. Current Sinking

The circuit shown in Figure 26 is used to test the current source capability, with the output clamped to around 5 V with a string of Zener diodes. The UCC27423 is found to source 4.8 A at V_{DD} = 15 V and 3.7 A at V_{DD} = 12 V.

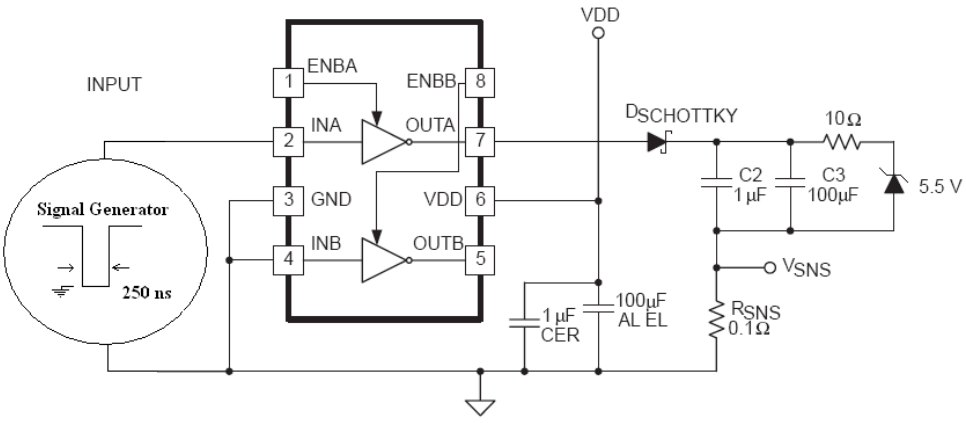


Figure 26. Current Sourcing

Note that the current sink capability is slightly stronger than the current source capability at lower V_{DD}. This is due to the differences in the structure of the bipolar-MOSFET power output section, where the current source is a P-channel MOSFET, and the current sink has an N-channel MOSFET.

In most applications, it is advantageous that the turn-off capability of a driver is stronger than the turn-on capability. This helps ensure that the MOSFET is held OFF during common power-supply transients, which may turn the device back ON.

8.2.2.2 Parallel Outputs

The A and B drivers may be combined into a single driver by connecting the INA/INB inputs together and the OUTA/OUTB outputs together. Then, a single signal can control the paralleled combination as shown in Figure 27.

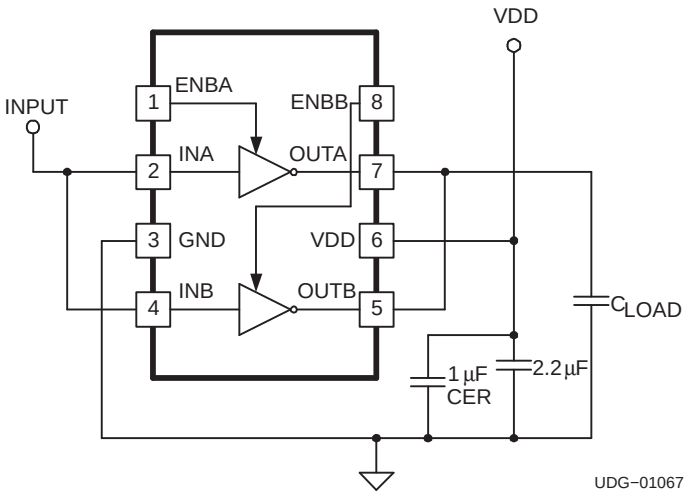


Figure 27. Parallel Outputs

8.2.3 Application Curve

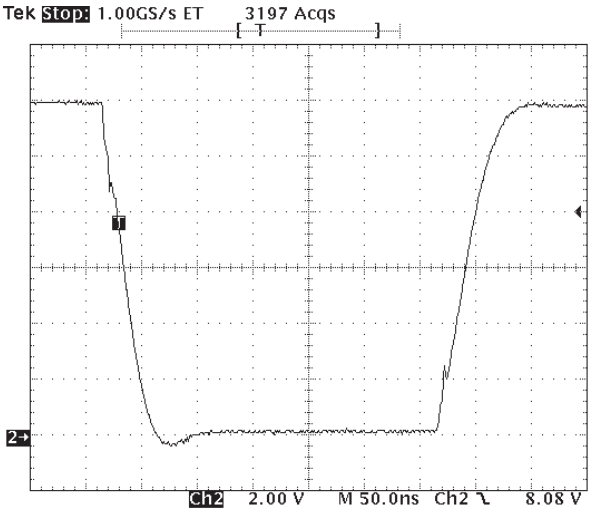


Figure 28. Pulse Response

9 Power Supply Recommendations

9.1 Drive Current and Power Requirements

The UCC2742x is capable of delivering 4 A of current to a MOSFET gate for a period of several-hundred nanoseconds. High-peak current is required to turn the device ON quickly. To turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. This discussion uses a MOSFET because it is the most common type of switching device used in high-frequency power-conversion equipment.

References (1) and (2) discuss the current required to drive a power MOSFET and other capacitive-input switching devices. Reference (2) includes information on the previous generation of bipolar IC gate drivers.

When a driver IC is tested with a discrete, capacitive load, it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 2.

$$E = \frac{1}{2}CV^2$$

where

- C is the load capacitor
- V is the bias voltage feeding the driver (2)

An equal amount of energy is transferred to ground when the capacitor is discharged. This leads to a power loss, given by Equation 3.

$$P = 2 \times \frac{1}{2}CV^2 f$$

where

- f is the switching frequency (3)

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as in Equation 4.

$$P = 10\ nF \times (12)^2 \times (300\ kHz) = 0.432\ W \quad (4)$$

With a 12-V supply, this equates to a current of:

$$I = \frac{P}{V} = \frac{0.432\ W}{12\ V} = 0.036\ A \quad (5)$$

The actual current measured from the supply was 0.037 A, and is very close to the predicted value. But, the I_{DD} current that is due to the IC internal consumption should be considered. With no load, the IC current draw is 0.0027 A. Under this condition, the output rise and fall times are faster than with a load. This could lead to an almost insignificant, yet measurable, current due to cross conduction in the output stages of the driver. However, these small current differences are buried in the high-frequency switching spikes and are beyond the measurement capabilities of a basic laboratory setup. The measured current with a 10-nF load is reasonably close to that which is predicted.

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance, plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge, Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence, Q_g = CeffV, to provide the following equation for power.

$$P = C \times V^2 \times f = Q_g \times f \quad (6)$$

Equation 6 allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

10 Layout

10.1 Layout Guidelines

Circuit layout is extremely critical in gate drive circuit. As shows in graphics below there might be considerable distance between the PWM controller and the MOSFET. This distance introduces parasitics inductance due to the loop formed by the gate drive and ground return trace, which can slow down the switching speed and can cause ringing at the gate drive waveform. To reduce the inductance linked to the gate drive connection, a wider PCB trace is desirable. Gate driver incorporates short propagation delays and powerful output stage capable of delivering large current peaks with fast rise and fall times at the gate of the power switch to facilitate voltage transition very quickly. Very high peak current result in high di/dt which can cause unacceptable ringing if the trace lengths and impedances are not well controlled.

- Locate the device driver as close as possible to power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD during turnon of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (driver device, power MOSFET and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances - during turn-on and turn-off transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible parallel the source and return traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch and ground of PWM controller at one point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

10.2 Layout Example

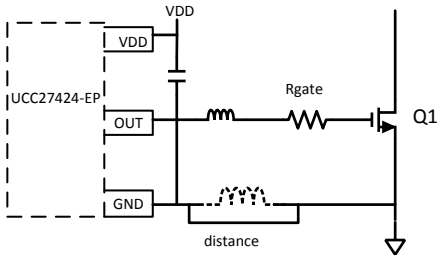


Figure 29. Noise Shielding Example Layout

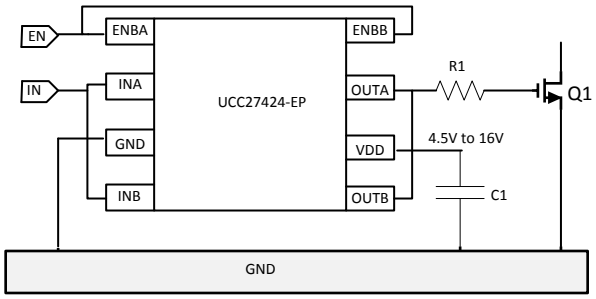


Figure 30. PCB Layout Example

10.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the IC package. For a power driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced, while keeping the junction temperature within rated limits.

As shown in *Power Dissipation Ratings*, the SOIC-8 (D) package has a power rating of around 0.5 W with T_A = 70°C. This limit is imposed in conjunction with the power derating factor also given in the table. Note that the power dissipation in the earlier example is 0.432 W with a 10-nF load, 12 VDD, switched at 300 kHz. Thus, only one load of this size could be driven using the D package, even if the two onboard drivers are paralleled. The difficulties with heat removal limit the drive available in the older packages.

The MSOP-8 PowerPAD (DGN) package significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As shown in reference (3), the PowerPAD packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PCB directly underneath the IC package, reducing the $R_{\theta JC}$ to 4.7°C/W. Data is presented in reference (3) to show that the power dissipation can be quadrupled in the PowerPAD package configuration when compared to the standard packages. The PCB must be designed with thermal lands and thermal vias to complete the heat-removal subsystem, as summarized in reference (4). This allows a significant improvement in heatsinking over that available in the D package and is shown to more than double the power capability of the D package. Note that the PowerPAD package is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

Table 3. Related Products

PRODUCT	DESCRIPTION	PACKAGES
UCC37324	Dual 4-A low-side drivers	MSOP-8 PowerPAD, SOIC-8, PDIP-8

11.2 Documentation Support

11.2.1 Related Documentation

(1) Power Supply Seminar SEM-1400 Topic 2: *Design and Application Guide For High-Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, SLUP133.

(2) Application note, *Practical Considerations in High-Performance MOSFET, IGBT, and MCT Gate Drive Circuits*, by Bill Andreycak, SLUA105.

(3) Technical brief, *PowerPad™ Thermally-Enhanced Package*, SLMA002.

(4) Application brief, *PowerPad™ Made Easy*, SLMA004.

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC27423-EP	Click here	Click here	Click here	Click here	Click here
UCC27424-EP	Click here	Click here	Click here	Click here	Click here

11.4 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27423MDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	27423EP	Samples
UCC27424MDGNREP	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	424E	Samples
V62/07624-01XE	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	424E	Samples
V62/07624-02YE	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	27423EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC27423-EP, UCC27424-EP :

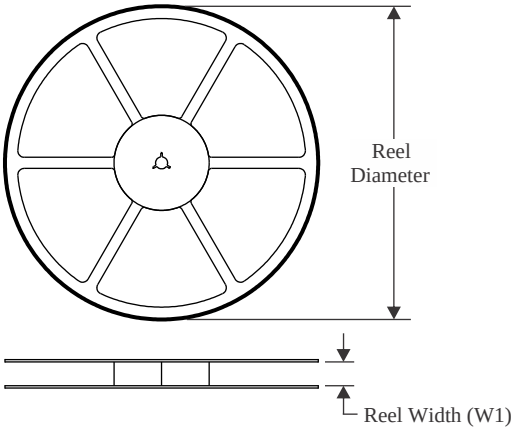
- Catalog: UCC27423, UCC27424
- Automotive: UCC27423-Q1, UCC27424-Q1

NOTE: Qualified Version Definitions:

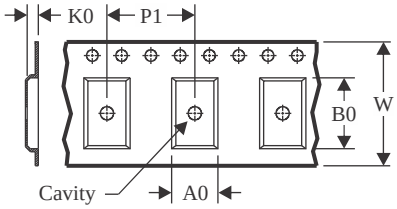
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

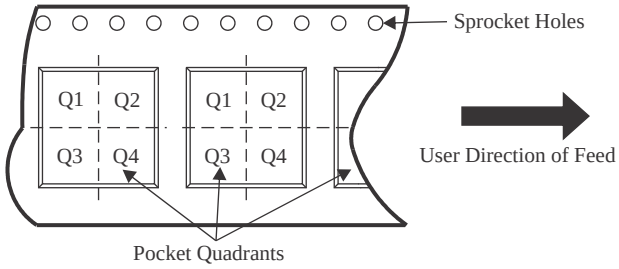


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

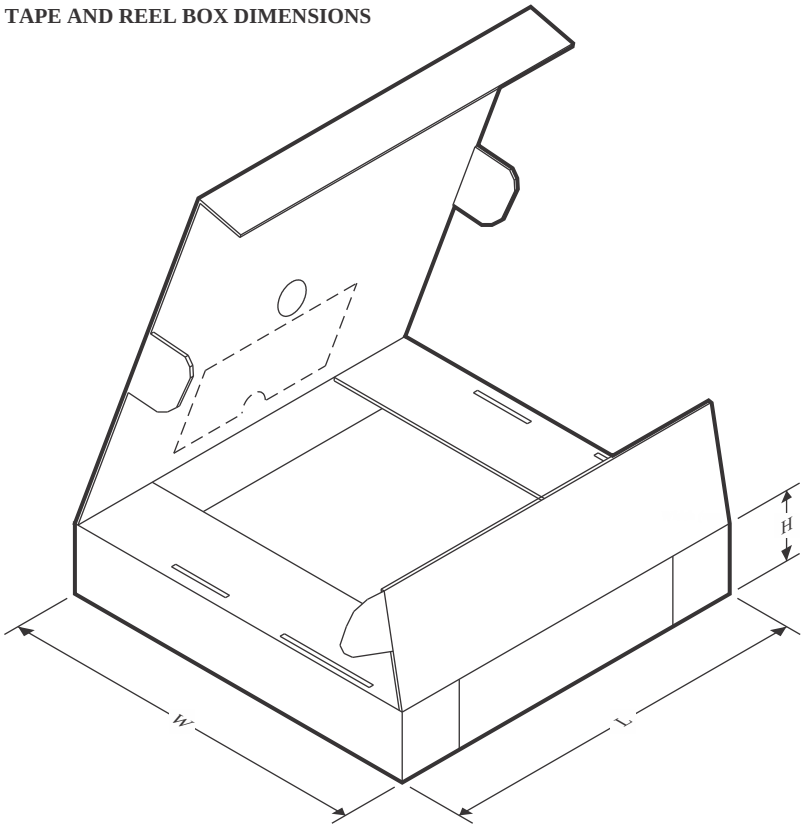
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27423MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27424MDGNREP	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27423MDREP	SOIC	D	8	2500	356.0	356.0	35.0
UCC27424MDGNREP	HVSSOP	DGN	8	2500	350.0	350.0	43.0

GENERIC PACKAGE VIEW

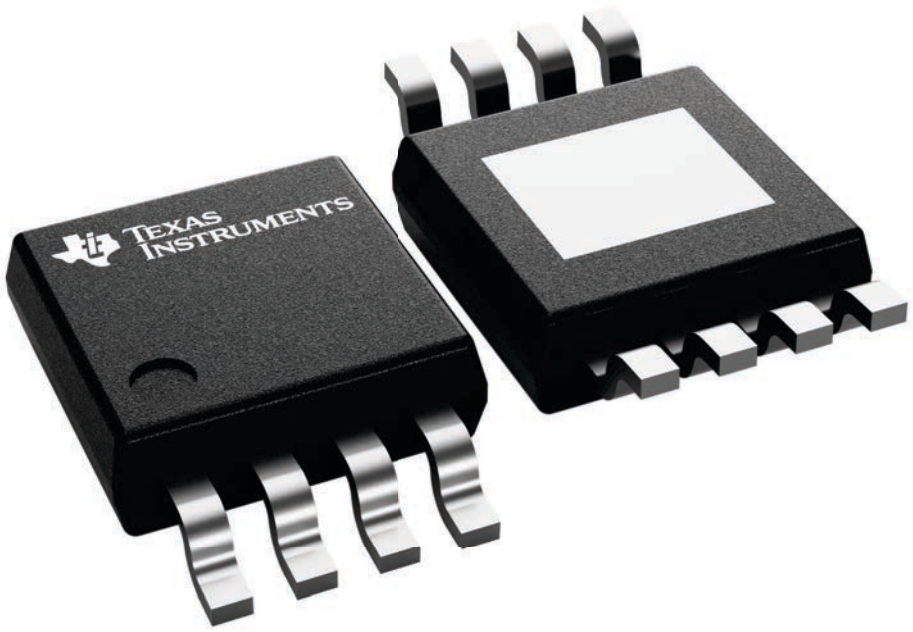
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

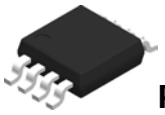
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

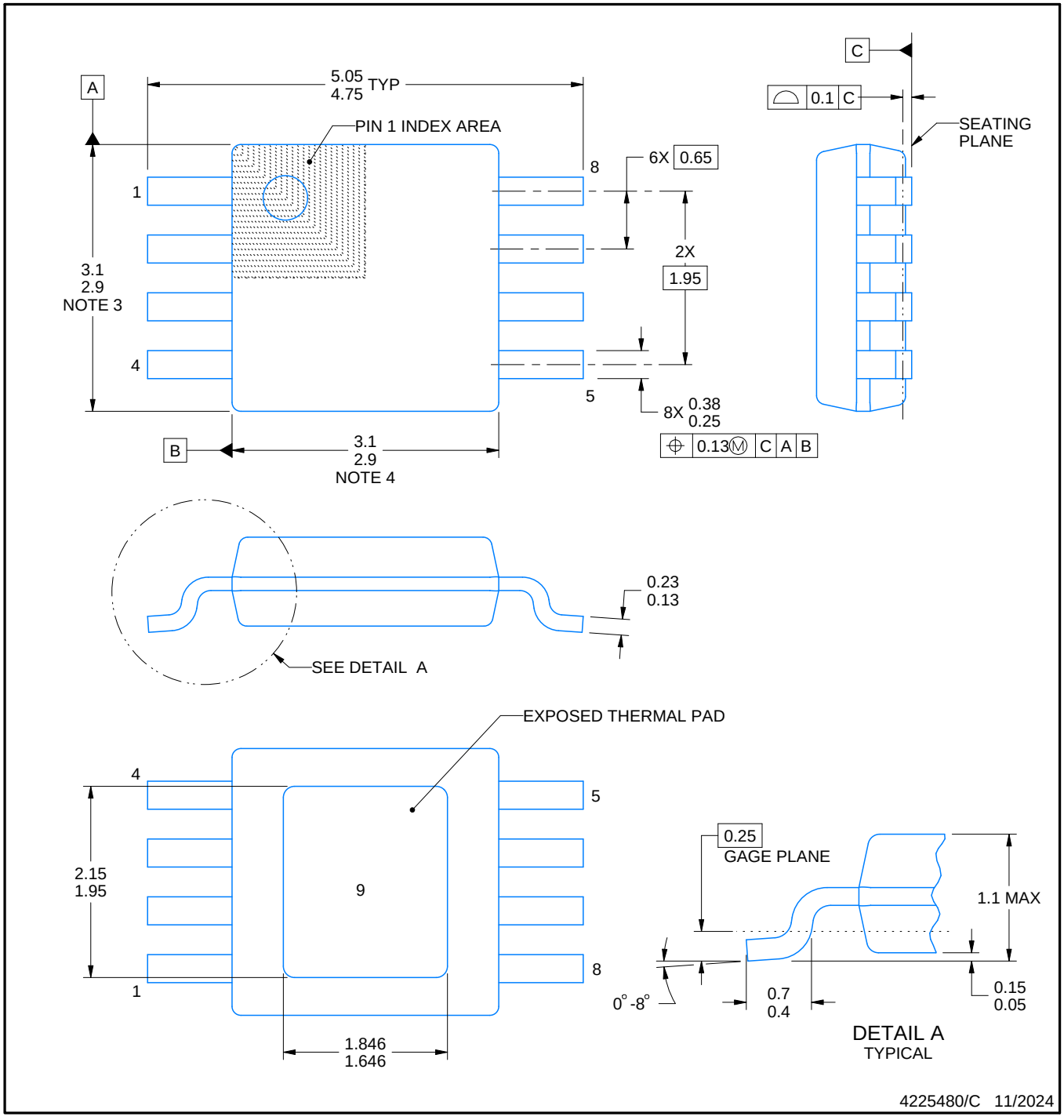
PACKAGE OUTLINE

DGN0008G



PowerPAD™ HVSSOP - 1.1 mm max height

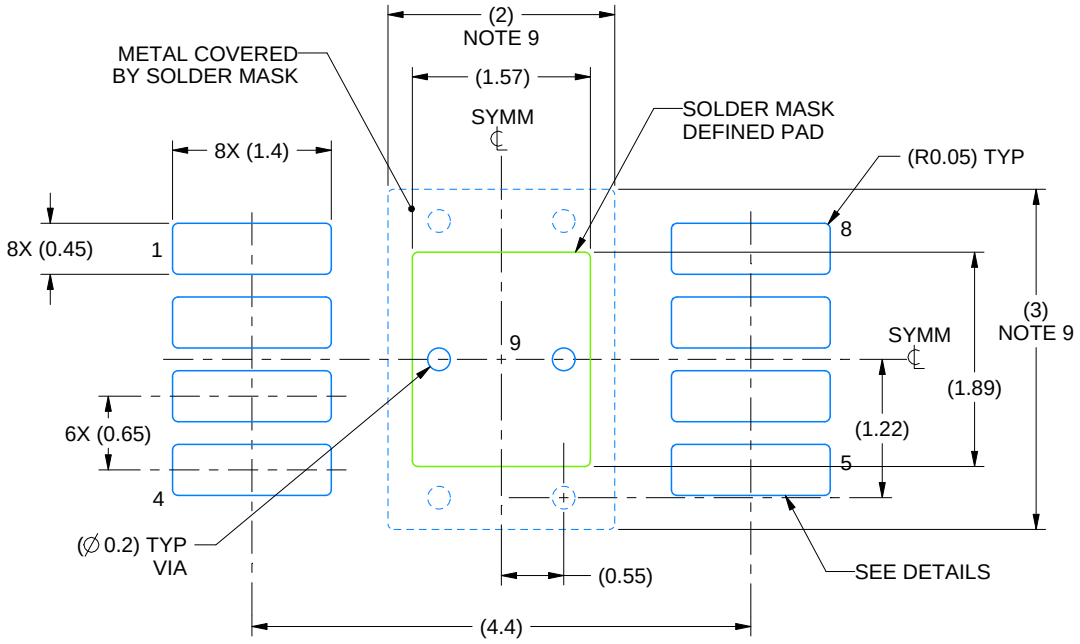
SMALL OUTLINE PACKAGE



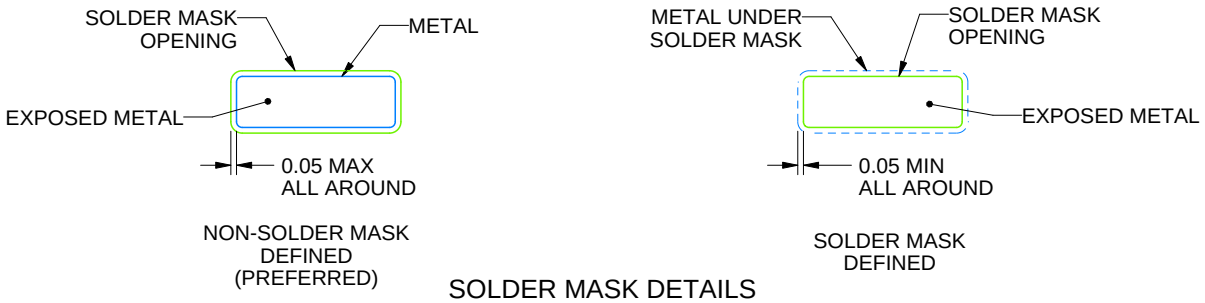
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

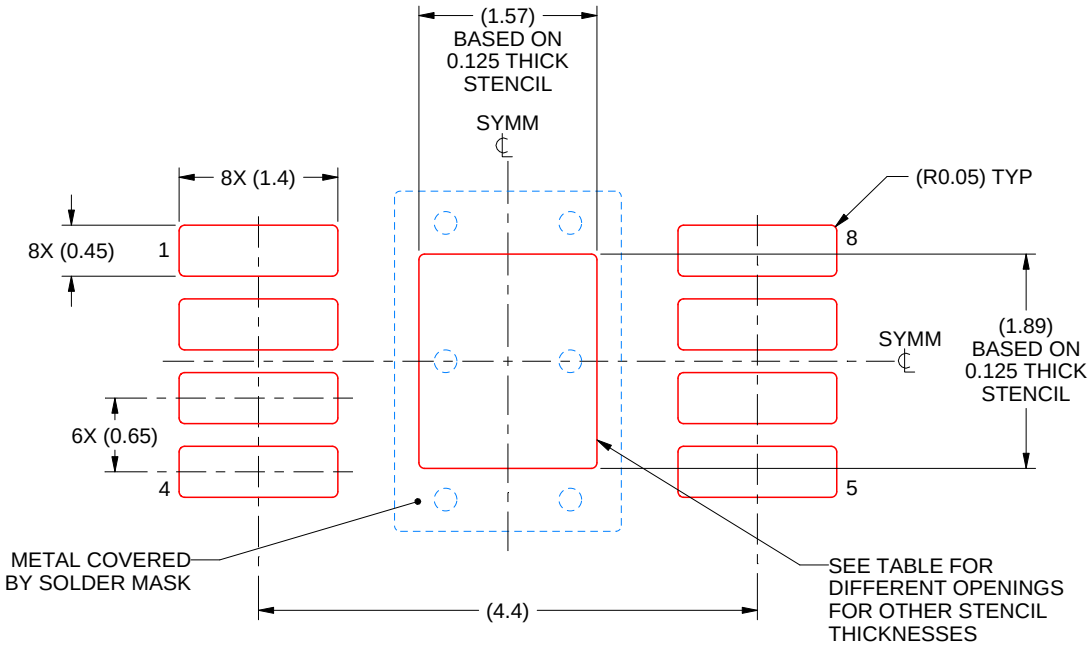


SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

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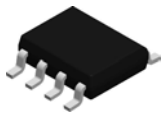
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

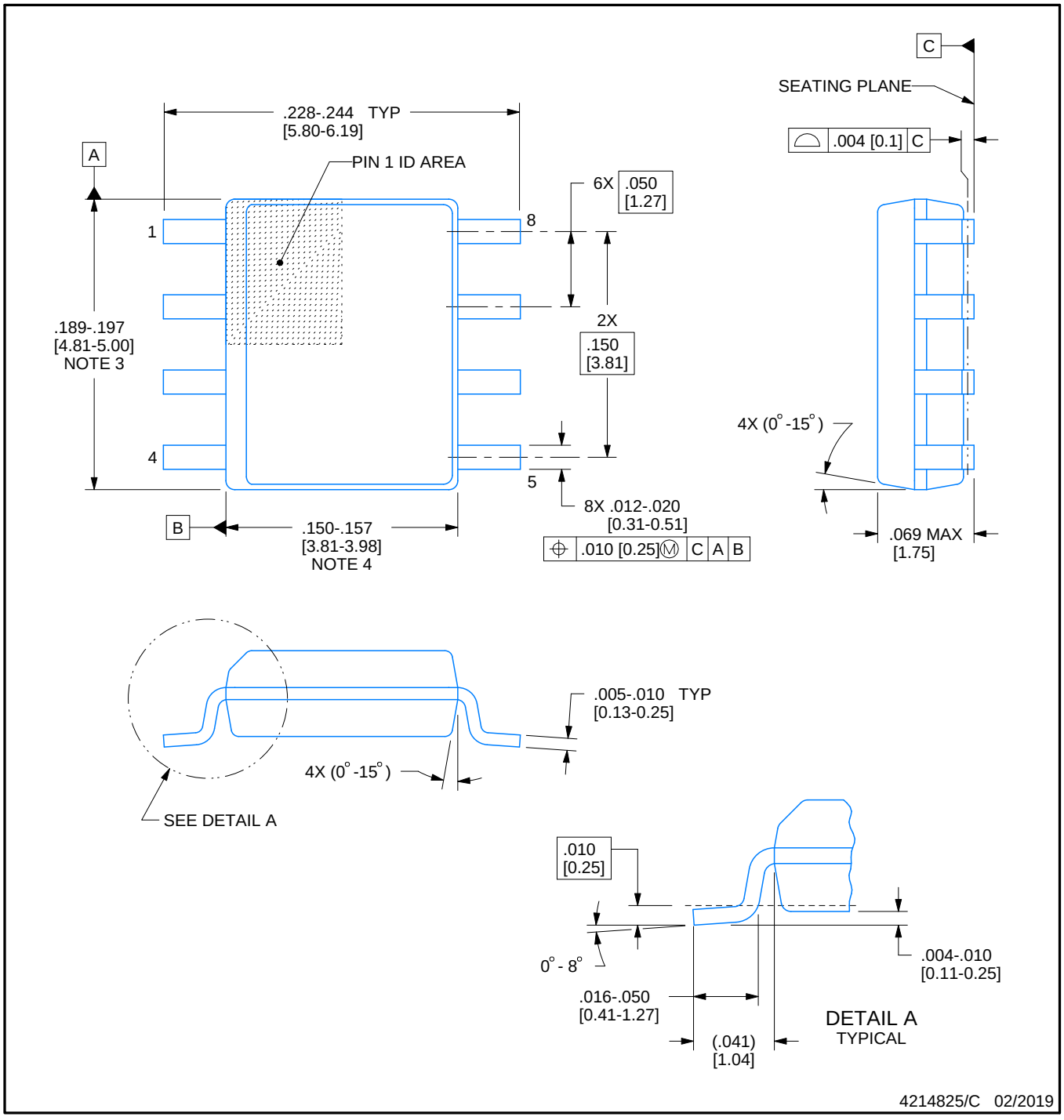


PACKAGE OUTLINE

D0008A

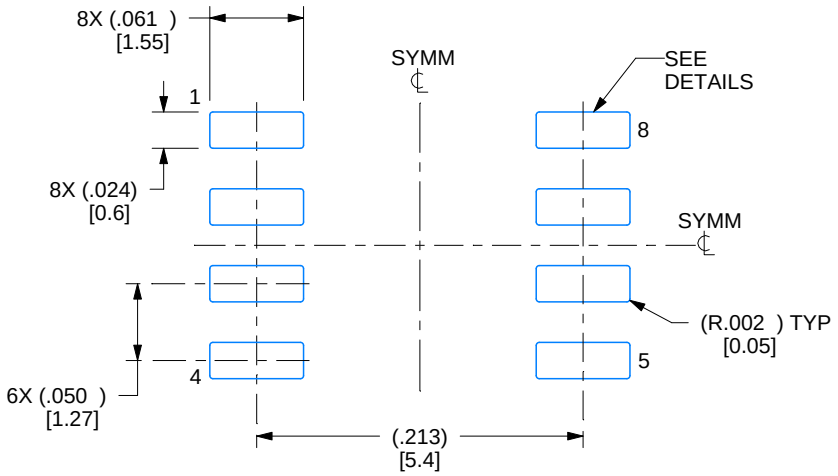
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

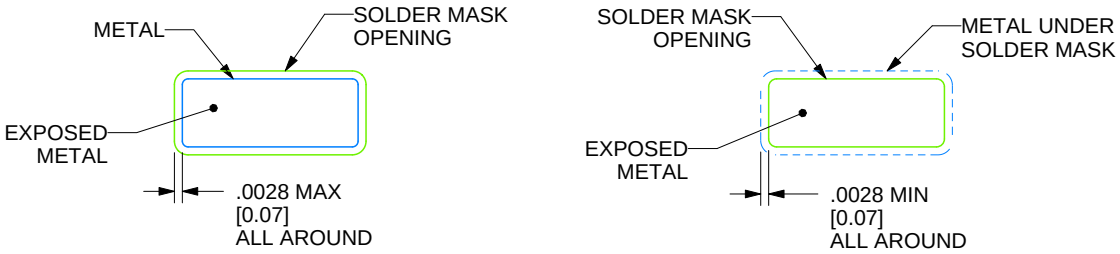


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

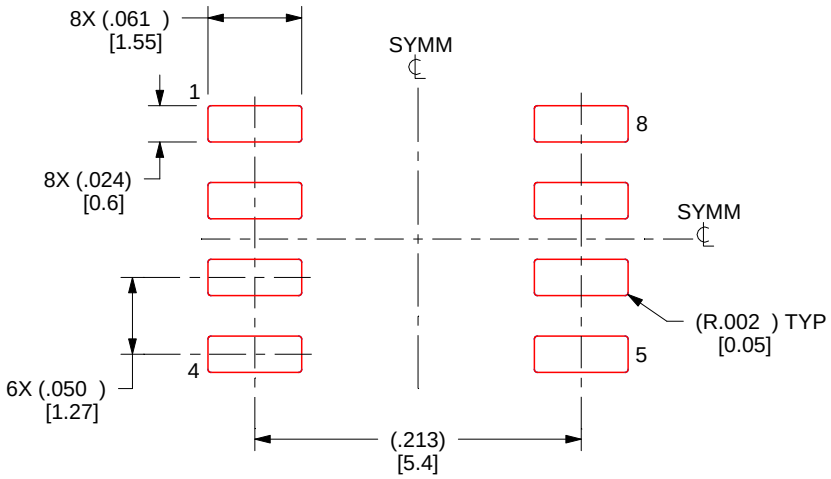
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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