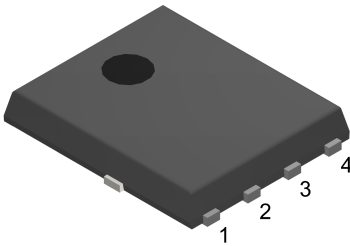
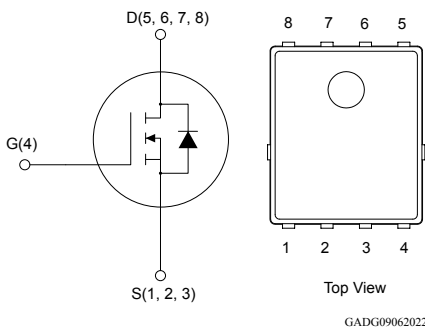


# N-channel logic level 40 V, 1.0 mΩ max., 304 A, STripFET F8 Power MOSFET in a PowerFLAT 5x6 package


**PowerFLAT 5x6**


## Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STL300N4LF8	40 V	1.0 mΩ	304 A

- MSL1 grade
- 175 °C maximum operating junction temperature
- 100% avalanche tested
- Low gate charge  $Q_g$

## Applications

- Industrial tools, motor drives and equipment
- Industrial motor control
- Power supplies and converters

## Description

The **STL300N4LF8** is a 40 V N-channel enhancement mode Power MOSFET designed in STripFET F8 technology featuring an enhanced trench gate structure.

It ensures a state-of-the-art of figure of merit for very low on-state resistance while reducing internal capacitances and gate charge for faster and more efficient switching.



### Product status link

[STL300N4LF8](#)

### Product summary

<b>Order code</b>	STL300N4LF8
<b>Marking<sup>(1)</sup></b>	300N4LF8
<b>Package</b>	PowerFLAT 5x6
<b>Packing</b>	Tape and reel

1. For engineering samples marking, see Section 3.3: PowerFLAT 5x6 marking information.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings (at  $T_C = 25\text{ °C}$  unless otherwise specified)**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}^{(2)}$	304	A
	Drain current (continuous) at $T_C = 100\text{ °C}^{(2)}$	215	
	Drain current (continuous) at $T_C = 25\text{ °C}^{(3)}$	120	
$I_{DM}^{(1)(2)(4)}$	Drain current (pulsed, $t_p = 10\text{ }\mu\text{s}$ )	1217	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ °C}$	167	W
$I_{AS}$	Single pulse avalanche current (pulse width limited by $T_J$ max.)	60	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$ , $I_D = 60\text{ A}$ , $R_{Gmin} = 25\text{ }\Omega$ )	420	mJ
$T_J$	Operating junction temperature range	-55 to 175	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range		$^{\circ}\text{C}$

1. Specified by design, not tested in production.
2. This is the theoretical current value only related to the silicon.
3. This current value is limited by package.
4. Pulse width is limited by safe operating area.

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient (on 2s2p FR-4 board vertical in still area)	16.5	$^{\circ}\text{C/W}$
$R_{thJC}$	Thermal resistance, junction-to-case max.	0.9	$^{\circ}\text{C/W}$

1. Defined according to JEDEC standards (JESD51-5, -7).

## 2 Electrical characteristics

$T_J = 25\text{ °C}$  unless otherwise specified.

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	40			V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 40\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 40\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ °C}^{(1)}$			100	
$I_{GSS}$	Gate-body leakage current	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1.2		2.0	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 60\text{ A}$		0.8	1.0	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 60\text{ A}$		1.15	1.5	
$R_G$	Gate resistance			1.0		$\Omega$

1. Specified by design and evaluated by characterization, not tested in production.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}^{(1)}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	5400	-	pF
$C_{oss}^{(1)}$	Output capacitance		-	1700	-	pF
$C_{rss}^{(1)}$	Reverse transfer capacitance		-	25	-	pF
$Q_g^{(1)}$	Total gate charge	$V_{DD} = 20\text{ V}$ , $I_D = 60\text{ A}$ , $V_{GS} = 0\text{ to }4.5\text{ V}$	-	30	-	nC
		$V_{DD} = 20\text{ V}$ , $I_D = 60\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$	-	70	-	
$Q_{gs}^{(1)}$	Gate-source charge	$V_{DD} = 20\text{ V}$ , $I_D = 60\text{ A}$ , $V_{GS} = 0\text{ to }4.5\text{ V}$	-	19	-	nC
$Q_{gd}^{(1)}$	Gate-drain charge		-	5	-	nC
$Q_{g(sync)}^{(1)}$	Total gate charge, sync. MOSFET	$V_{DS} = 0.1\text{ V}$ , $V_{GS} = 0\text{ to }4.5\text{ V}$	-	63	-	nC
$Q_{oss}^{(1)}$	Output charge	$V_{DD} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$	-	75	-	nC

1. Specified by design and evaluated by characterization, not tested in production.

**Table 5. Switching times**

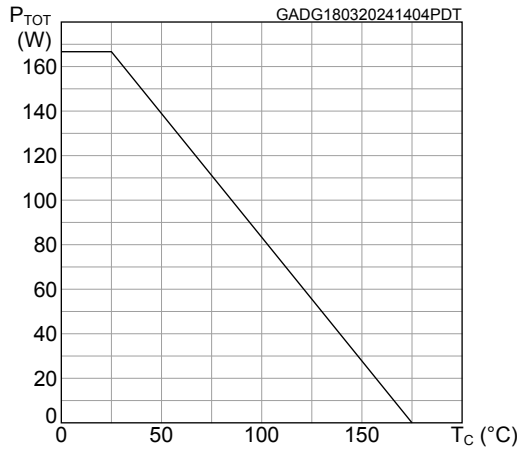
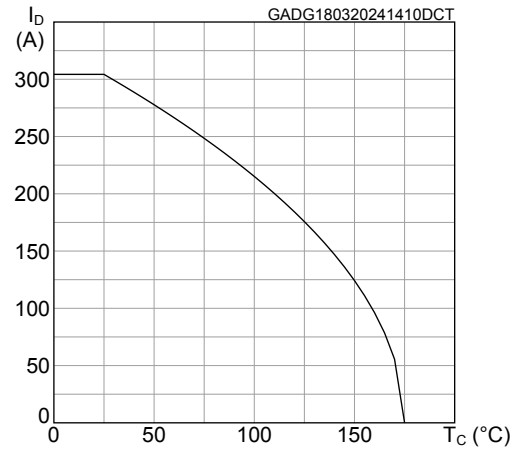
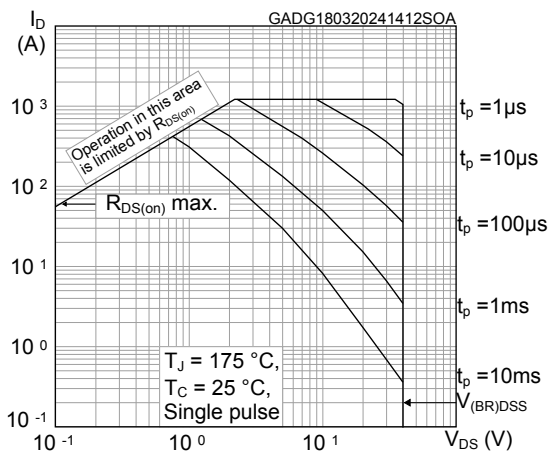
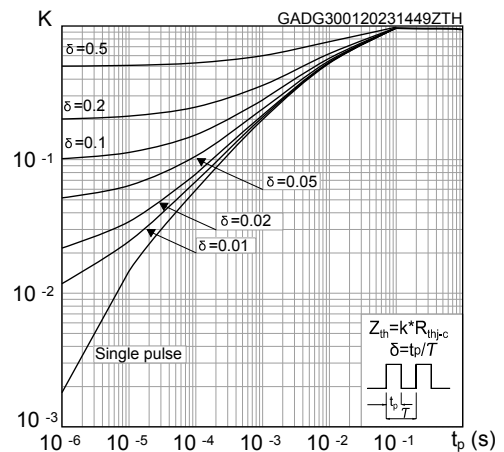
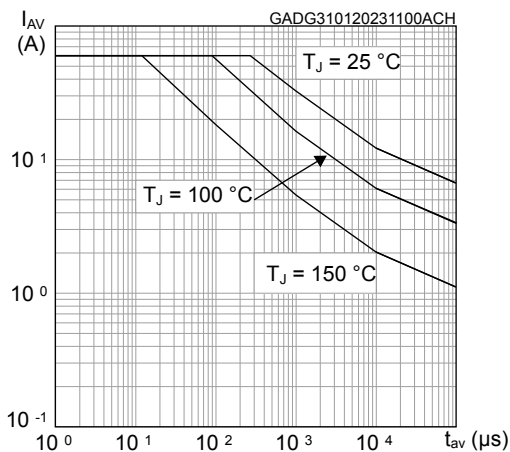
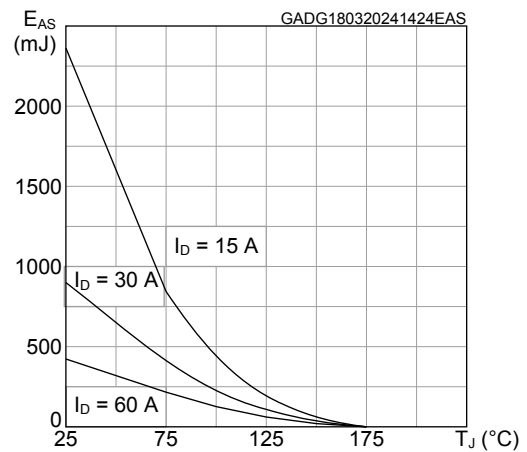
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}^{(1)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$ , $I_D = 60\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	14	-	ns
$t_r^{(1)}$	Rise time		-	6	-	ns
$t_{d(off)}^{(1)}$	Turn-off delay time		-	55	-	ns
$t_f^{(1)}$	Fall time		-	9	-	ns

1. Specified by design and evaluated by characterization, not tested in production.

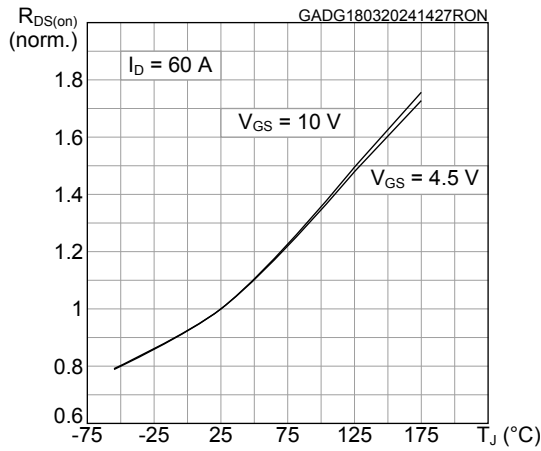
**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)(2)}$	Forward on current (continuous)	$T_C = 25\text{ °C}$	-		121	A
$V_{SD}$	Forward on voltage	$I_{SD} = 60\text{ A}, V_{GS} = 0\text{ V}$	-		1.1	V
$t_{rr}^{(1)}$	Reverse recovery time	$I_D = 60\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 32\text{ V}$	-	60		ns
$Q_{rr}^{(1)}$	Reverse recovery charge		-	70		nC
$I_{RRM}^{(1)}$	Reverse recovery current		-	2.5		A

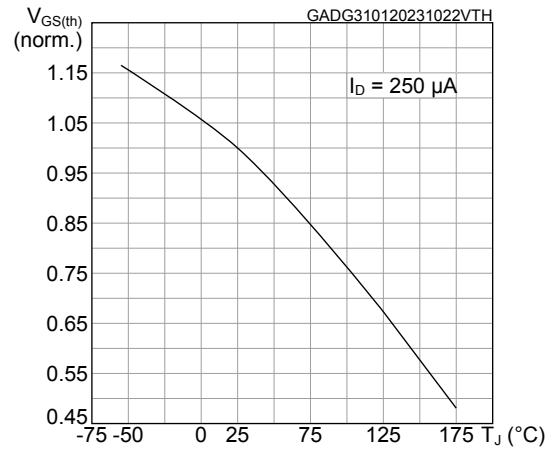
1. Specified by design and evaluated by characterization, not tested in production.
2. This is the theoretical current value only related to the silicon.

**2.1 Electrical characteristics (curves)**
**Figure 1. Total power dissipation**

**Figure 2. Drain current vs case temperature**

**Figure 3. Safe operating area**

**Figure 4. Normalized transient thermal impedance**

**Figure 5. Avalanche characteristics**

**Figure 6. Avalanche energy**


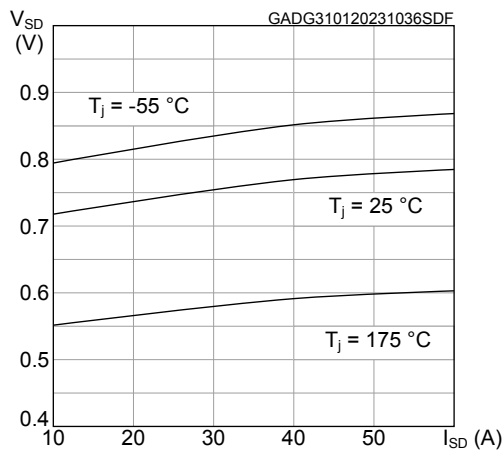
**Figure 7. Normalized on-resistance vs temperature**



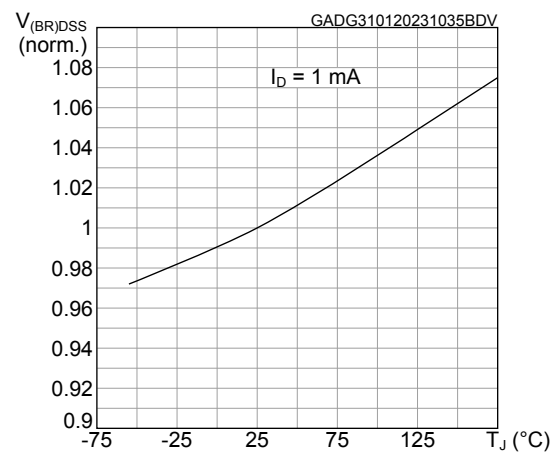
**Figure 8. Normalized gate threshold voltage vs temperature**



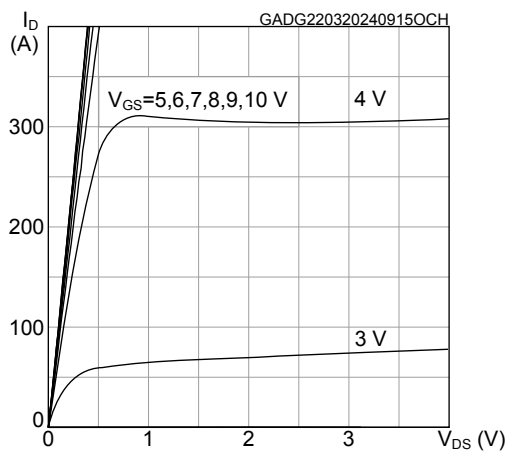
**Figure 9. Typical reverse diode forward characteristics**



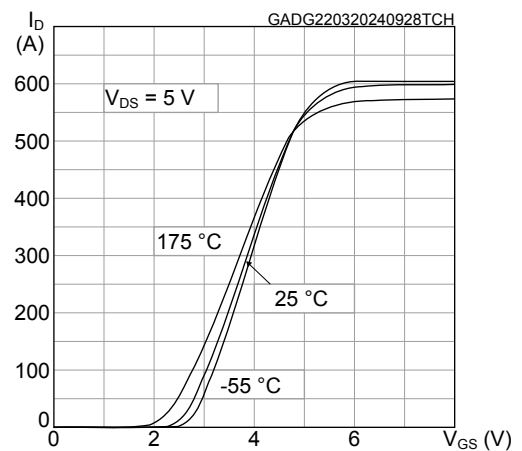
**Figure 10. Normalized  $V_{(BR)DSS}$  vs temperature**



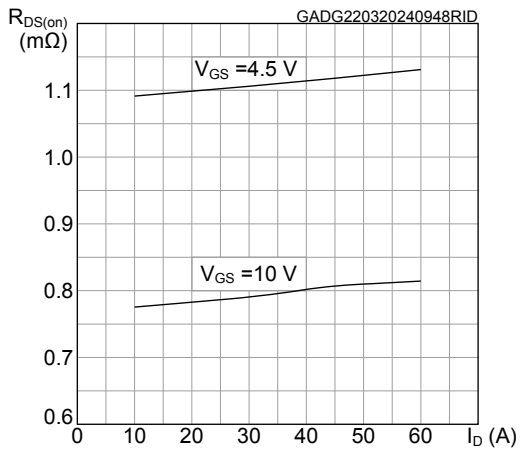
**Figure 11. Typical output characteristics**



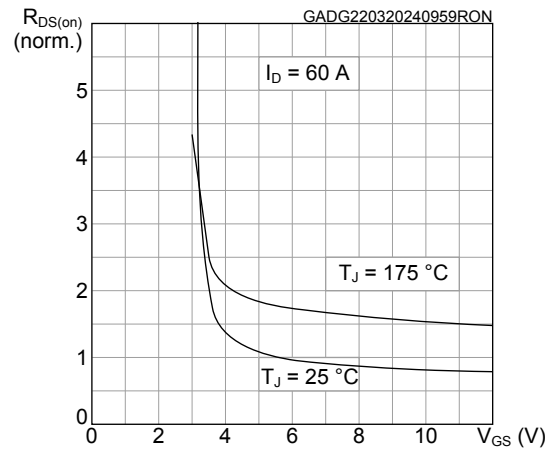
**Figure 12. Typical transfer characteristics**



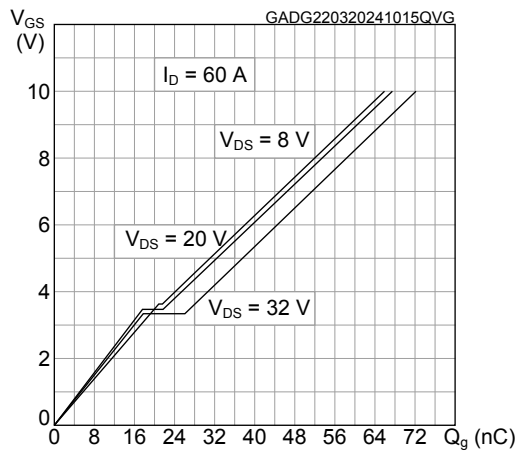
**Figure 13. Typical drain-source on-resistance**



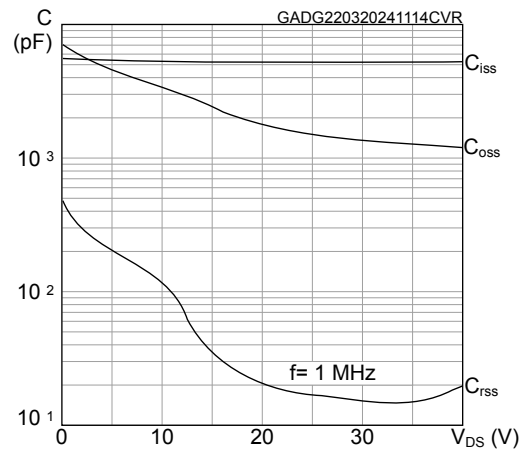
**Figure 14. Typical on-resistance vs gate-source voltage**



**Figure 15. Typical gate charge characteristics**



**Figure 16. Typical capacitance characteristics**

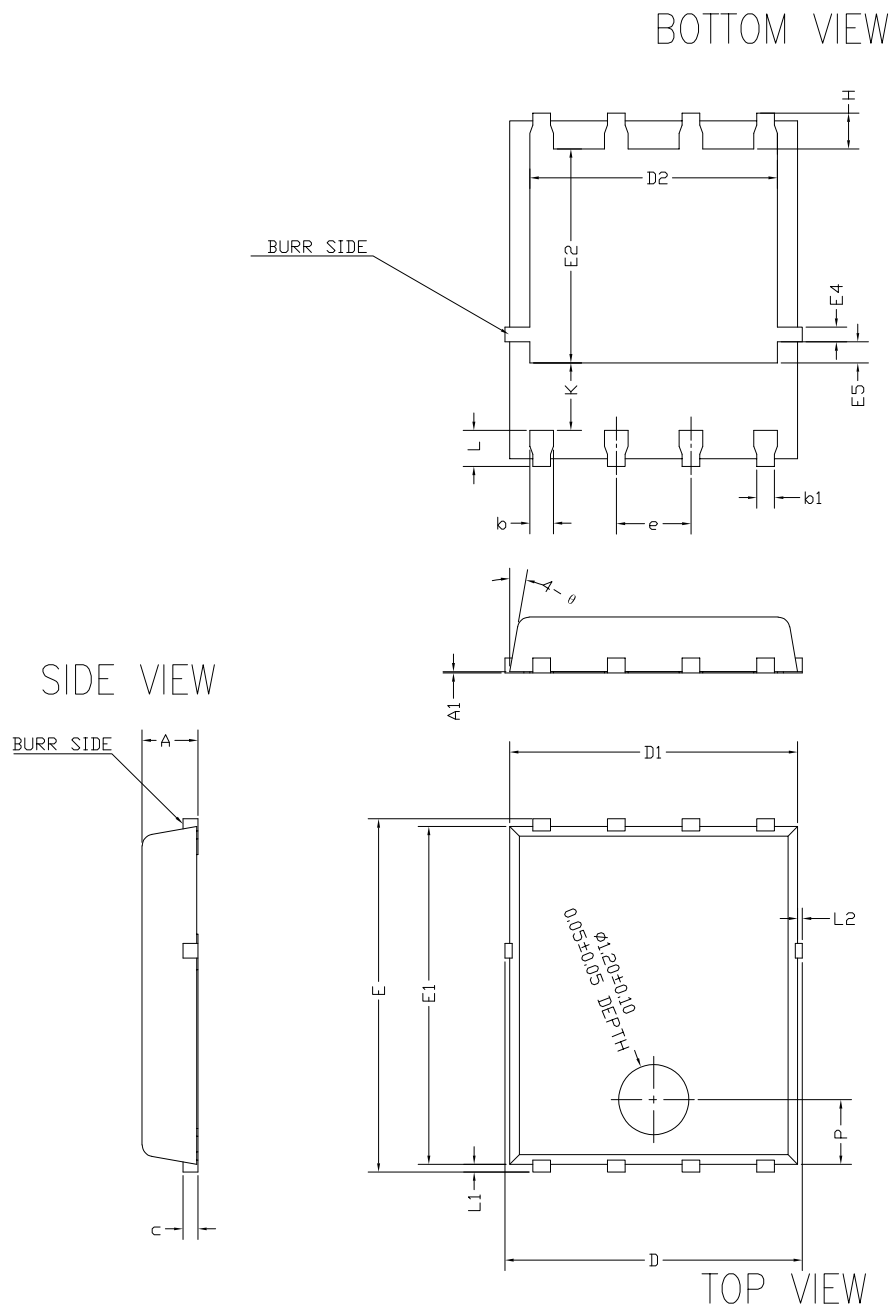


### 3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

#### 3.1 PowerFLAT 5x6 type B package information

Figure 17. PowerFLAT 5x6 type B package outline



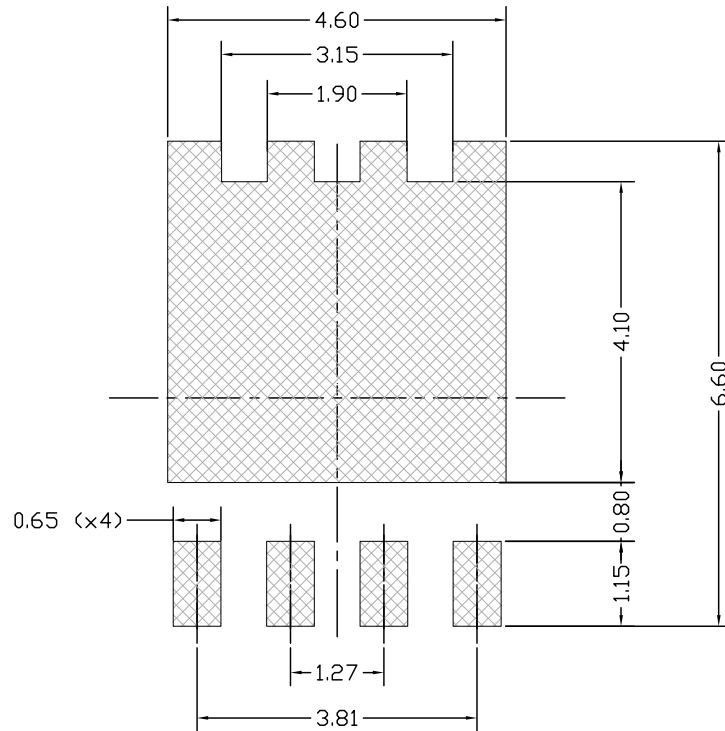
Drawing\_8472137\_typeB rev5



**Table 7. PowerFLAT 5x6 type B mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1		0.02	
b	0.35	0.40	0.45
b1		0.30	
c	0.21	0.25	0.34
D	4.80		5.10
D1	4.80	4.90	5.00
D2	4.01	4.21	4.31
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.54	3.64	3.74
E4	0.15	0.25	0.35
E5	0.26	0.36	0.46
H	0.51	0.61	0.71
K	0.95		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
$\theta$	8°	10°	12°

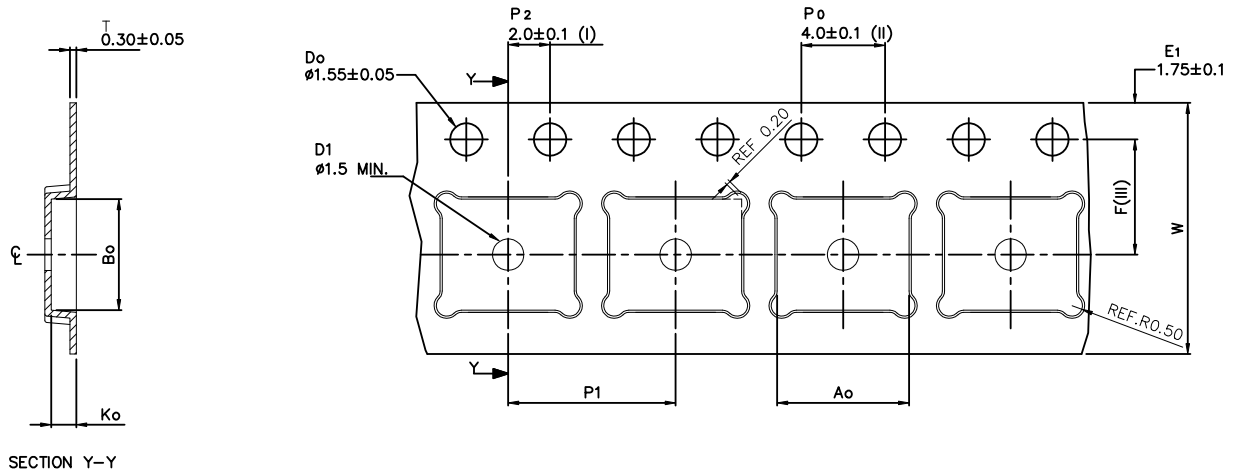
**Figure 18. PowerFLAT 5x6 recommended footprint (dimensions are in mm)**



Footprint\_8472137\_typeB rev5

### 3.2 PowerFLAT 5x6 packing information

**Figure 19. PowerFLAT 5x6 tape (dimensions are in mm)**



Ao	6.30	+/- 0.1
Bo	5.30	+/- 0.1
Ko	1.20	+/- 0.1
F	5.50	+/- 0.1
P1	8.00	+/- 0.1
W	12.00	+/- 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .

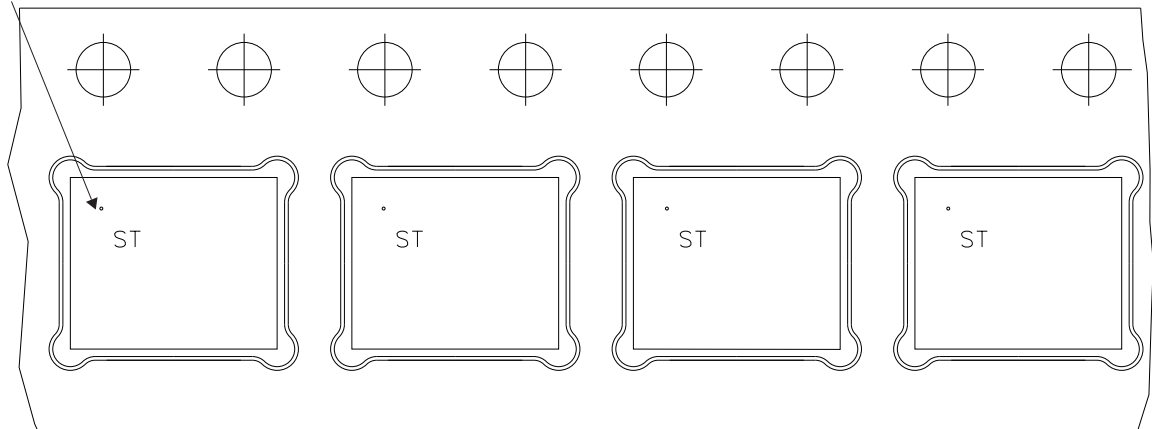
(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs  
All dimensions are in millimeters

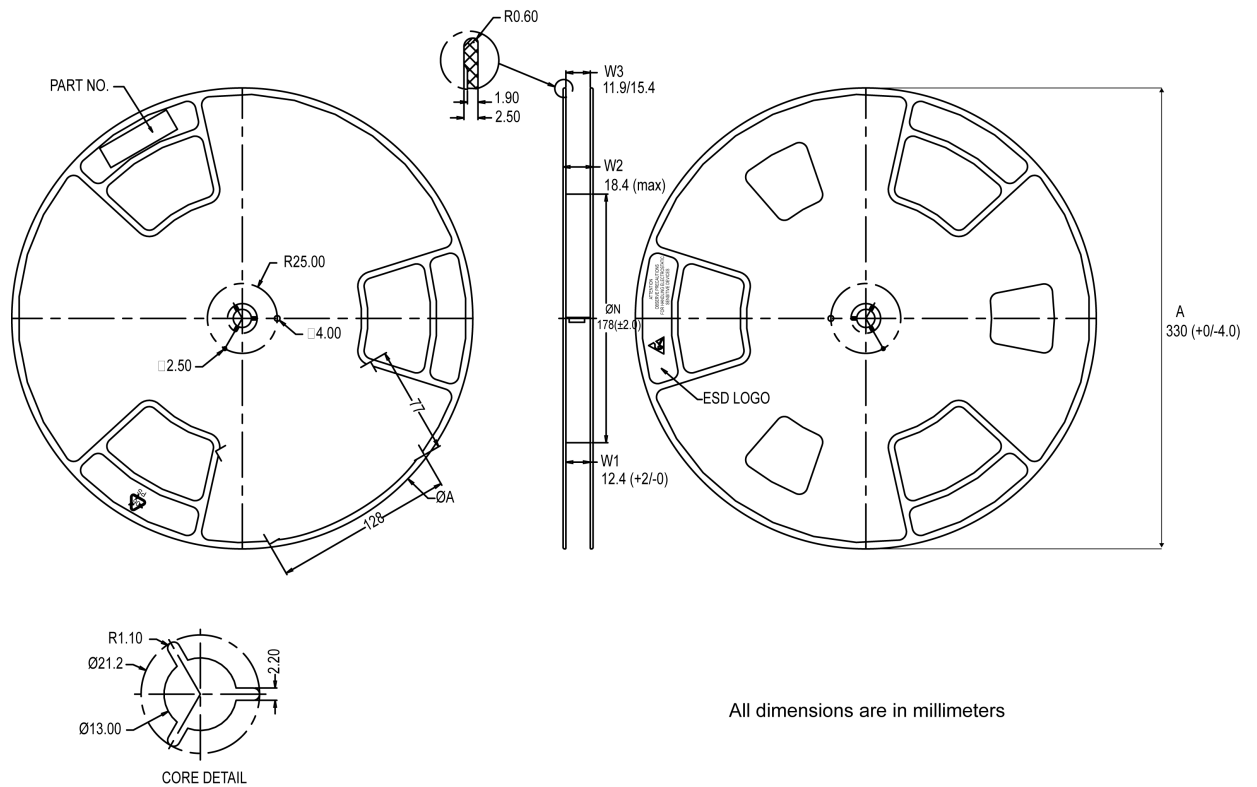
8234350\_Tape\_rev\_C

**Figure 20. PowerFLAT 5x6 package orientation in carrier tape**

Pin 1 identification



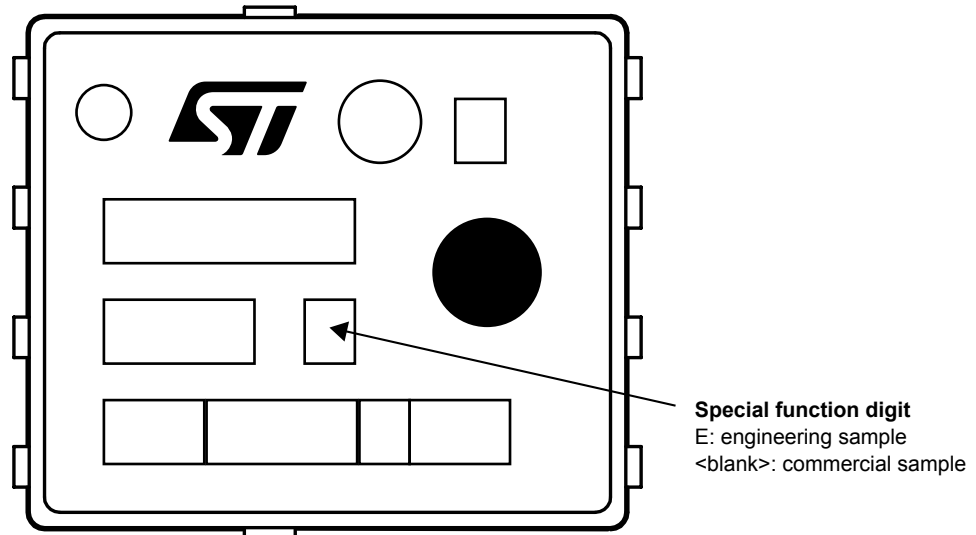
**Figure 21. PowerFLAT 5x6 reel**



8234350\_Reel\_rev\_C

### 3.3 PowerFLAT 5x6 marking information

Figure 22. PowerFLAT 5x6 marking information



**Note:** *Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.*

Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.

## Revision history

**Table 8. Document revision history**

Date	Revision	Changes
03-Feb-2023	1	Initial release.
02-Apr-2024	2	<p>Updated Features, Applications and Description.</p> <p>Updated Section 1: Electrical ratings, Section 2: Electrical characteristics and Section 2.1: Electrical characteristics (curves).</p> <p>Added Figure 11. Typical output characteristics, Figure 12. Typical transfer characteristics, Figure 13. Typical drain-source on-resistance , Figure 15. Typical gate charge characteristics and Figure 16. Typical capacitance characteristics .</p>

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