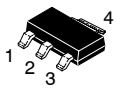
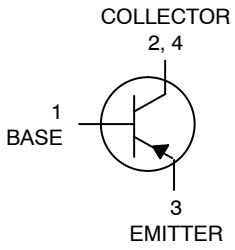
PNP Silicon Epitaxial Transistor

PZT2907A



SOT−223
CASE 318E
STYLE 1



This PNP Silicon Epitaxial transistor is designed for use in linear and switching applications. The device is housed in the SOT-223 package which is designed for medium power surface mount applications.

Features

- NPN Complement is PZT2222AT1
- The SOT-223 Package can be Soldered Using Wave or Reflow
- SOT-223 Package Ensures Level Mounting, Resulting in Improved Thermal Conduction, and Allows Visual Inspection of Soldered Joints. The Formed Leads Absorb Thermal Stress during Soldering Eliminating the Possibility of Damage to the Die
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	−60	Vdc
Collector − Base Voltage	V_{CBO}	−60	Vdc
Emitter − Base Voltage	V_{EBO}	−5.0	Vdc
Collector Current − Continuous	I_C	−600	mAdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

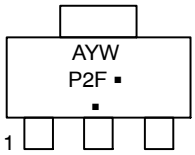
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation (Note 1) T_A = 25°C	P_D	1.5 12	W mW/°C
Thermal Resistance Junction−to−Ambient (Note 1)	$R_{\theta JA}$	83.3	°C/W
Lead Temperature for Soldering, 0.0625″ from case Time in Solder Bath	T_L	 260 10	 °C Sec
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to +150	°C

1. FR−4 with 1 oz and 713 mm^2 of copper area.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MARKING DIAGRAM



P2F = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
PZT2907AT1G	SOT−223 (Pb−Free)	1,000 / Tape & Reel
SPZT2907AT1G	SOT−223 (Pb−Free)	1,000 / Tape & Reel
PZT2907AT3G	SOT−223 (Pb−Free)	4,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Base Breakdown Voltage (I_C = −10 μAdc, I_E = 0)		$V_{(BR)CBO}$	−60	–	–	Vdc
Collector−Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)		$V_{(BR)CEO}$	−60	–	–	Vdc
Emitter−Base Breakdown Voltage (I_E = −10 μAdc, I_C = 0)		$V_{(BR)EBO}$	−5.0	–	–	Vdc
Collector−Base Cutoff Current (V_{CB} = −50 Vdc, I_E = 0)		I_{CBO}	–	–	−10	nAdc
Collector−Emitter Cutoff Current (V_{CE} = −30 Vdc, V_{BE} = 0.5 Vdc)		I_{CEX}	–	–	−50	nAdc
Base−Emitter Cutoff Current (V_{CE} = −30 Vdc, V_{BE} = −0.5 Vdc)		I_{BEX}	–	–	−50	nAdc
ON CHARACTERISTICS (Note 2)						
DC Current Gain (I_C = −0.1 mAdc, V_{CE} = −10 Vdc) (I_C = −1.0 mAdc, V_{CE} = −10 Vdc) (I_C = −10 mAdc, V_{CE} = −10 Vdc) (I_C = −150 mAdc, V_{CE} = −10 Vdc) (I_C = −500 mAdc, V_{CE} = −10 Vdc)		h_{FE}	 75 100 100 100 50	 – – – – –	 – – – 300 –	–
Collector-Emitter Saturation Voltages (I_C = −150 mAdc, I_B = −15 mAdc) (I_C = −500 mAdc, I_B = −50 mAdc)		$V_{CE(sat)}$	 – –	 – –	 −0.4 −1.6	Vdc
Base-Emitter Saturation Voltages (I_C = −150 mAdc, I_B = −15 mAdc) (I_C = −500 mAdc, I_B = −50 mAdc)		$V_{BE(sat)}$	 – –	 – –	 −1.3 −2.6	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain − Bandwidth Product (I_C = −50 mAdc, V_{CE} = −20 Vdc, f = 100 MHz)		f_T	200	–	–	MHz
Output Capacitance (V_{CB} = −10 Vdc, I_E = 0, f = 1.0 MHz)		C_c	–	–	8.0	pF
Input Capacitance (V_{EB} = −2.0 Vdc, I_C = 0, f = 1.0 MHz)		C_e	–	–	30	pF
SWITCHING TIMES						
Turn-On Time	(V_{CC} = −30 Vdc, I_C = −150 mAdc, I_{B1} = −15 mAdc)	t_{on}	–	–	45	ns
Delay Time		t_d	–	–	10	
Rise Time		t_r	–	–	40	
Turn-Off Time	(V_{CC} = −6.0 Vdc, I_C = −150 mAdc, I_{B1} = I_{B2} = −15 mAdc)	t_{off}	–	–	100	ns
Storage Time		t_s	–	–	80	
Fall Time		t_f	–	–	30	

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

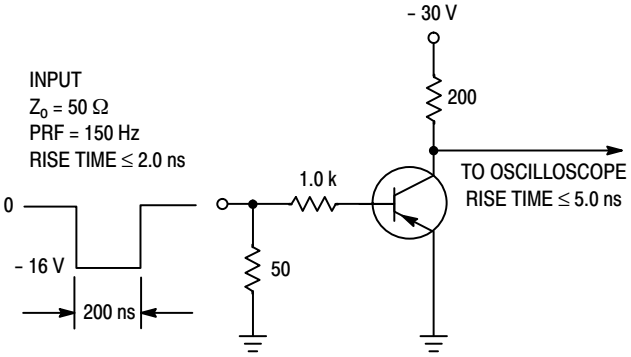


Figure 1. Delay and Rise Time Test Circuit

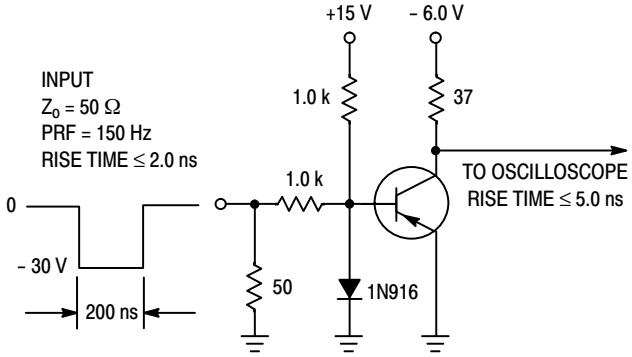


Figure 2. Storage and Fall Time Test Circuit

TYPICAL ELECTRICAL CHARACTERISTICS

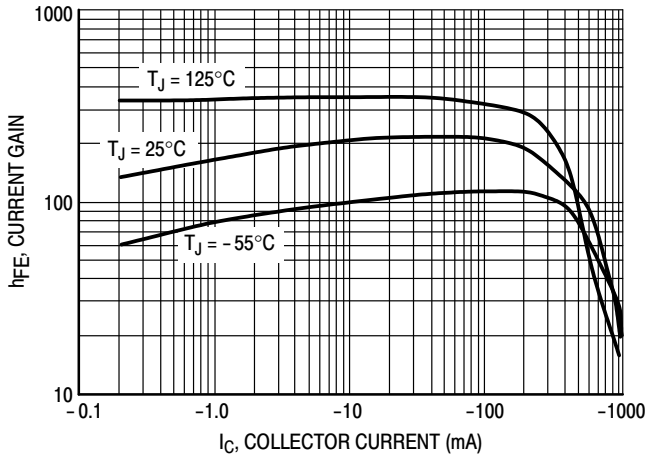


Figure 3. DC Current Gain

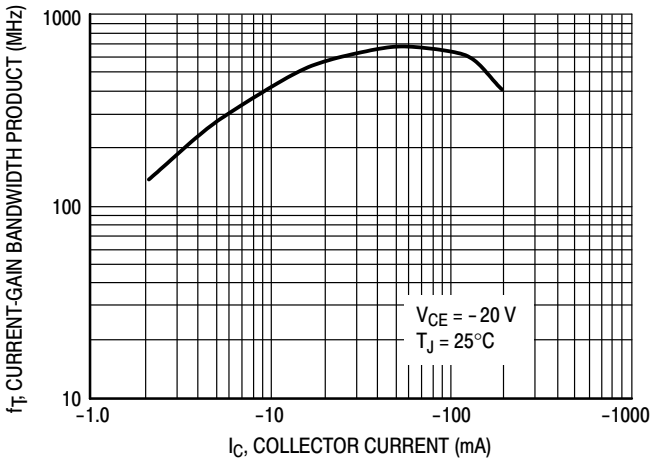


Figure 4. Current Gain Bandwidth Product

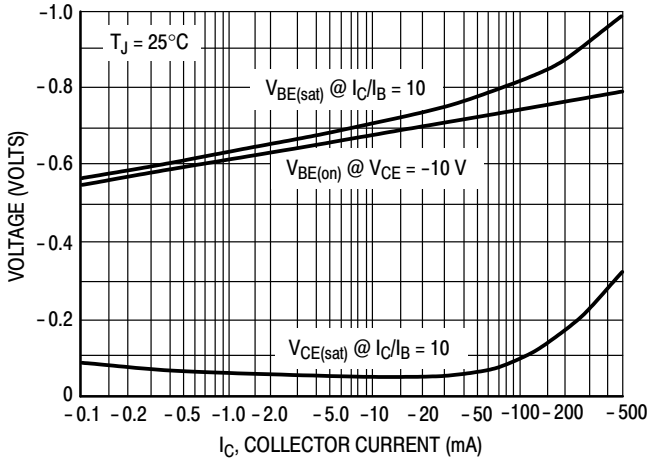


Figure 5. "ON" Voltage

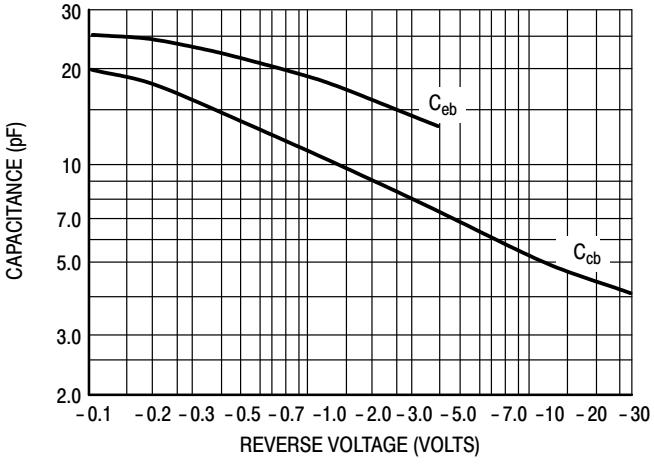
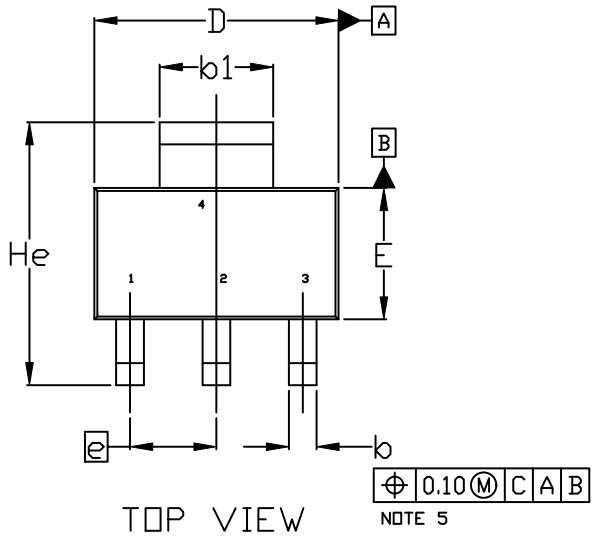


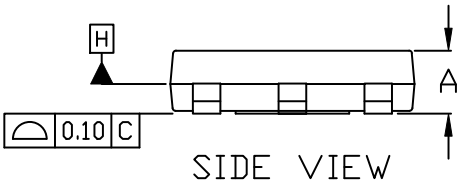
Figure 6. Capacitances

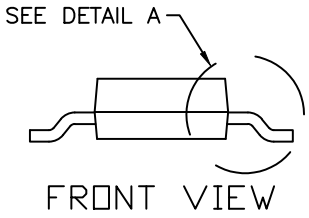
SCALE 1:1

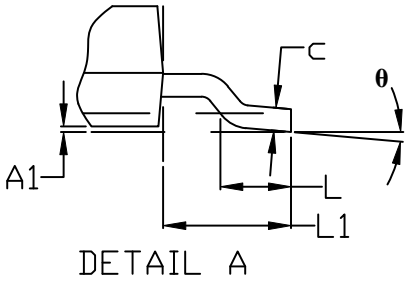
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



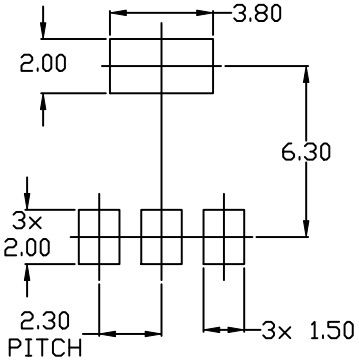






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

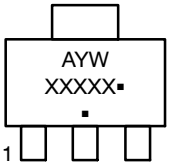
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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