

MOSFET - Power, Single N-Channel, DUAL COOL® 40 V, 0.78 mΩ, 310 A

NTMFSCOD8NO4XM

Features

- Dual Sided Cooling Package
- Latest 40 V Power MOSFET Technology for Motor Drive Applications
- Extreme Lower On–Resistance to Minimize Conduction Losses
- Lower Gate Charge to Minimize Gate Driving and Switching Losses
- Soft Body Diode Reverse Recovery
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

Applications

- Motor Drive
- ORing FET
- Battery Protection

MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V _{DSS}	40	V
Gate-to-Source Voltage	DC	V _{GS}	±20	V
Continuous Drain Current	T _C = 25°C	I _D	310	Α
(Note 2)	T _C = 100°C		219	
Power Dissipation (Note 2)	Power Dissipation (Note 2) $T_C = 25^{\circ}C$		135	W
Pulsed Drain Current $ \begin{array}{c} T_C = 25^{\circ}C, \\ t_p = 10 \; \mu s \end{array} $		I _{DM}	1463	Α
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +175	°C
Continuous Source-Drain Current (Body Diode)		I _S	150	Α
Single Pulse Avalanche Energy (I _{PK} = 69 A)		E _{AS}	248	mJ
Lead Temperature Soldering Purposes (1/8" from case for 10 s)		TL	260	°C

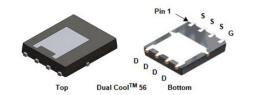
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

THERMAL CHARACTERISTICS

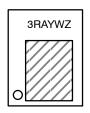
Symbol	Parameter	Max	Unit
$R_{ heta JC}$	Junction-to-Case (Bottom) - Steady State (Note 2)	1.1	°C/W
$R_{ heta JC}$	Junction-to-Case (Top) - Steady State (Note 2)	1.7	
$R_{\theta JA}$	Junction-to-Ambient - Steady State (Notes 1, 2)	39	

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
40 V	0.78 mΩ @ 10 V	310 A



DFN8 5x6 CASE 506EG

MARKING DIAGRAM



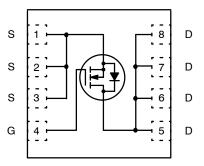
3R = Specific Device Code A = Assembly Location

Y = Year

W = Work Week

Z = Assembly Lot Code

N-Channel MOSFET



ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
OFF CHARACTERISTICS			•	•	•	•	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	40			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\frac{\Delta V_{(BR)DSS}}{\Delta T_J}$	I _D = 1 mA, Referenced to 25°C		15		mV/°C	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, T _J = 25°C			10	μΑ	
	T T	V _{DS} = 40 V, T _J = 125°C			100		
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA	
ON CHARACTERISTICS (Note 3)			•	•			
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 50 A		0.63	0.78	mΩ	
	l t	$V_{GS} = 7 \text{ V}, I_D = 50 \text{ A}$		0.86	1.25		
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D = 180 \mu A$	2.5	3.0	3.5	V	
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/ \Delta T_J$	$V_{GS} = V_{DS}$, $I_D = 180 \mu A$		-7		mV/°C	
Forward Trans-conductance	9FS	V _{DS} = 5 V, I _D = 50 A		244		S	
CHARGES & CAPACITANCES			•	•	•	•	
Input Capacitance	C _{ISS}	$V_{GS} = 0 \text{ V}, V_{DS} = 20 \text{ V}, f = 1 \text{ MHz}$		4651		pF	
Output Capacitance	C _{OSS}			3319		1	
Reverse Transfer Capacitance	C _{RSS}			69			
Output Charge	Q _{OSS}			100		nC	
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = 10 \text{ V}, V_{DD} = 20 \text{ V}, I_D = 50 \text{ A}$	1	72		1	
Threshold Gate Charge	Q _{G(TH)})		14]	
Gate-to-Source Charge	Q_{GS}			21		1	
Gate-to-Drain Charge	Q_{GD}			13		1	
Gate Plateau Voltage	V_{GP}			4.5		V	
Gate Resistance	R_{G}	f = 1 MHz	1	0.65	1.2	Ω	
SWITCHING CHARACTERISTICS (Not	e 3)					-	
Turn-On Delay Time	t _{d(ON)}	Resistive Load		28		ns	
Rise Time	t _r	V_{GS} = 0/10 V, V_{DD} = 20 V, I_{D} = 50 A, R_{G} = 2.5 Ω		10		1	
Turn-Off Delay Time	t _{d(OFF)}			45		1	
Fall Time	t _f			9.5		1	
SOURCE-TO-DRAIN DIODE CHARAC	TERISTICS		•	•			
Forward Diode Voltage	V_{SD}	$V_{GS} = 0 \text{ V}, I_S = 50 \text{ A}, T_J = 25^{\circ}\text{C}$		0.81	1.2	V	
		V _{GS} = 0 V, I _S = 50 A, T _J = 125°C		0.66 1.0	1		
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V}, \text{ dI}_{S}/\text{dt} = 100 \text{ A}/\mu\text{s},$		69		ns	
Charge Time	ta	$I_S = 50 \text{ A}, V_{DD} = 50 \text{ V}$		36		1	
Discharge Time	t _b			33		1	
Reverse Recovery Charge	Q _{RR}			144		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

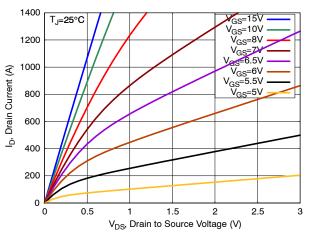


Figure 1. On-Region Characteristics

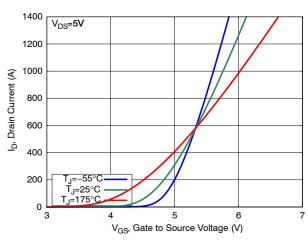


Figure 2. Transfer Characteristics

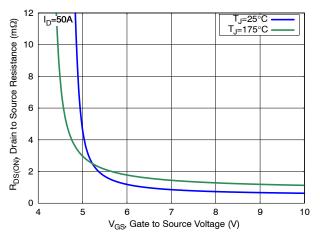


Figure 3. On-Resistance vs. Gate Voltage

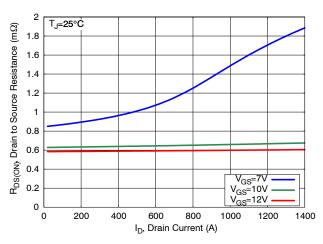


Figure 4. On-Resistance vs. Drain Current

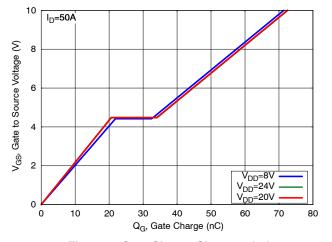


Figure 5. Gate Charge Characteristics

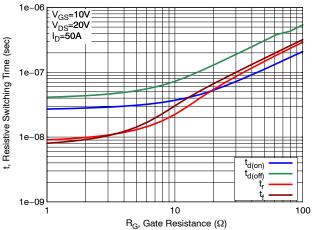
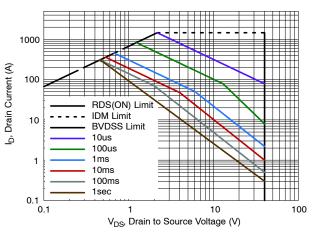


Figure 6. Resistive Switching Time Variation vs. Gate Resistance

TYPICAL CHARACTERISTICS



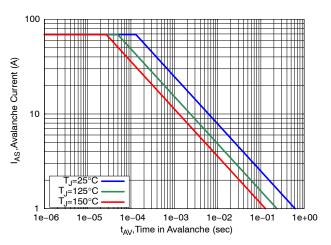


Figure 7. Safe Operating Area (SOA)

Figure 8. Avalanche Current vs Pulse Time (UIS)

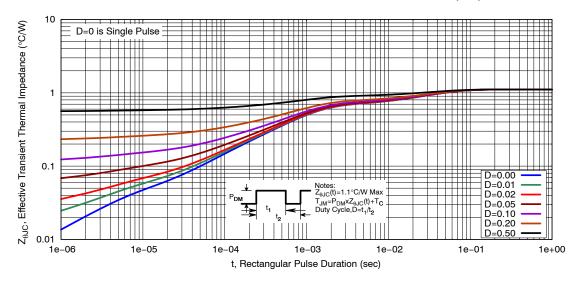


Figure 9. Transient Thermal Response

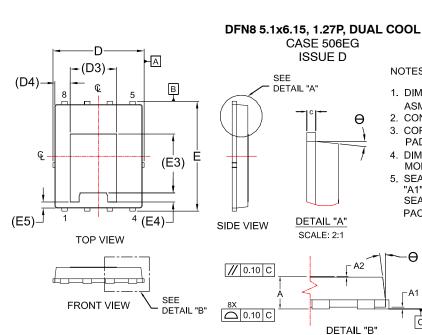
ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
NTMFSC0D8N04XMTWG	3R	DFN8 5x6 (Pb–Free/Halogen Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS



0.10**M** C A B 0.05**M** C

1/2e

-b1 (8X) b (4X)

Κ

E1 E2

le

(E6

NOTES:

Θ

С

SEATING PI ANF

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
_ Divi	MIN.	NOM.	MAX.
Α	0.85 0.90 (0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
С	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
Е	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3		3.30 REF	•
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
е	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
١	0.56	0.66	0.76
L1	0.52	0.62	0.72
Φ	0°		12°

SCALE: 2:1
5.10
3.75
1.27 KEEP OUT AREA
1.27 0.61
LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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