

MOSFET - Power, Single N-Channel, SUPERFET[®], with Zener Diode, DPAK 600 V, 280 m Ω , 13 A NTD280N60S5Z

Description

SUPERFET V MOSFET Easy Drive series combines excellent switching performance without sacrificing ease of use and EMI issues for both hard and soft switching topologies.

Features

- 650 V @ $T_J = 150$ °C, Typ.
- $R_{DS(on)} = 224 \text{ m}\Omega$
- 100% Avalanche Tested
- Pb-Free, Halogen Free / BFR Free and are RoHS Compliant

Applications

- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Lighting / Charger / Adapter / Industrial Power Supplies

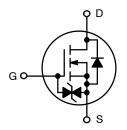
ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	600	V
Gate-to-Source Voltage	DC	V_{GS}	±20	V
	AC (f > 1 Hz)		±20	
Continuous Drain Current	T _C = 25°C	I _D	13	Α
	T _C = 100°C		8	
Power Dissipation	T _C = 25°C	P_{D}	89	W
Pulsed Drain Current (Note 1)	T _C = 25°C	I _{DM}	39	Α
Pulsed Source Current (Body Diode) (Note 1)		I _{SM}	39	Α
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C
Source Current (Body Diode)		IS	13	Α
Single Pulse Avalanche Energy	$I_L = 2.9 A$ $R_G = 25 \Omega$	E _{AS}	82	mJ
Avalanche Current		I _{AS}	2.9	Α
Repetitive Avalanche Energy (Note 1)		E _{AR}	0.89	mJ
MOSFET dv/dt		dv/dt	120	V/ns
Peak Diode Recovery dv/dt (Note 2)			50	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. $I_{SD} \le 5.5$ A, di/dt ≤ 200 A/s, $V_{DD} \le 400$ V, starting $T_J = 25$ °C.

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
600 V	280 m Ω @ V _{GS} = 10 V	13 A



N-CHANNEL MOSFET



MARKING DIAGRAM



T280N60S5Z = Specific Device Code

A = Assembly Location

Y = Year WW = Work Week ZZ = Lot Code

ORDERING INFORMATION

Device	Package	Shipping [†]
NTD280N60S5Z	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

^{*}Drain current limited by maximum junction temperature.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{ heta JC}$	1.4	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	52	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
OFF CHARACTERISTICS				•		
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}, T_J = 25^{\circ}\text{C}$	600	-	-	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	ΔV _{(BR)DSS} / ΔT _J	I _D = 10 mA, Referenced to 25°C	-	630	-	mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 600 V, T _J = 25°C	-	-	1	μΑ
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	±5	μΑ
ON CHARACTERISTICS						
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 5.5 A, T _J = 25°C	-	224	280	mΩ
Gate Threshold Voltage	V _{GS(th)}	$V_{GS} = V_{DS}$, $I_D = 1$ mA, $T_J = 25$ °C	2.4	-	4	V
Forward Trans-conductance	9FS	V _{DS} = 20 V, I _D = 5.5 A	-	10.6	-	S
CHARGES, CAPACITANCES & GATE	RESISTANCE					
Input Capacitance	C _{ISS}	$V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V}, f = 250 \text{ kHz}$	-	978	-	pF
Output Capacitance	C _{OSS}		-	16.8	-	-
Time Related Output Capacitance	C _{OSS(tr)}	I_D = Constant, V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	276	-	
Energy Related Output Capacitance	C _{OSS(er)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	-	30.5	-	
Total Gate Charge	Q _{G(TOT)}	V _{DD} = 400 V, I _D = 5.5 A, V _{GS} = 10 V	-	17.9	-	nC
Gate-to-Source Charge	Q _{GS}		-	4.53	-	
Gate-to-Drain Charge	Q_{GD}		-	4.8	-	
Gate Resistance	R_{G}	f = 1 MHz	-	5.11	-	Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	t _{d(ON)}	$V_{GS} = 0/10 \text{ V}, V_{DD} = 400 \text{ V},$	-	15.5	-	ns
Rise Time	t _r	$I_D = 5.5 \text{ A}, R_G = 12 \Omega$	-	4.27	-	
Turn-Off Delay Time	t _{d(OFF)}		-	52	-	
Fall Time	t _f		-	4.53	-	
SOURCE-TO-DRAIN DIODE CHARAC	TERISTICS					
Forward Diode Voltage	V_{SD}	I _{SD} = 5.5 A, V _{GS} = 0 V, T _J = 25°C	-	_	1.2	V
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, I _{SD} = 5.5 A,	-	229	-	ns
Reverse Recovery Charge	Q _{RR}	dI/dt = 100 A/μs, V _{DD} = 400 V	_	2114	_	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

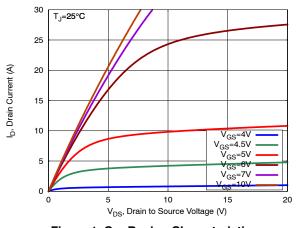


Figure 1. On-Region Characteristics

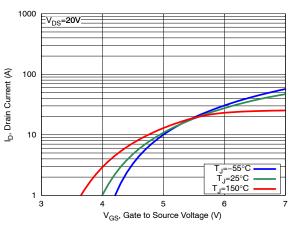


Figure 2. Transfer Characteristics

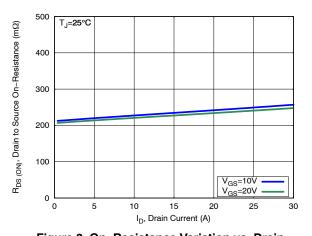


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

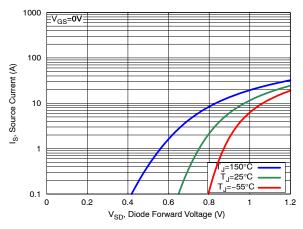


Figure 4. Diode Forward Voltage vs. Source Current

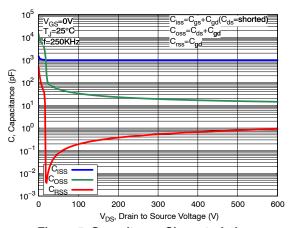


Figure 5. Capacitance Characteristics

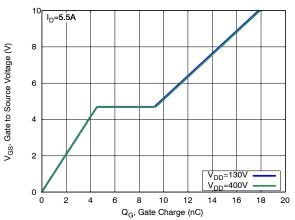


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

ID, Drain Current (A)

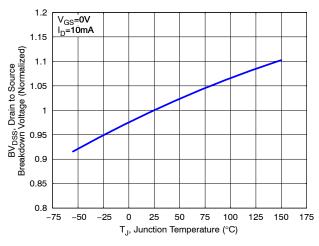


Figure 7. Breakdown Voltage Variation vs. Temperature

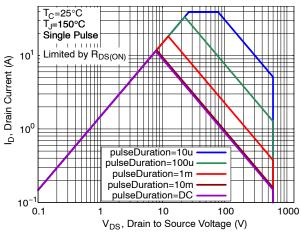


Figure 9. Maximum Safe Operating Area

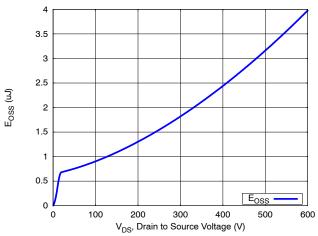


Figure 11. Eoss vs. Drain-to-Source Voltage

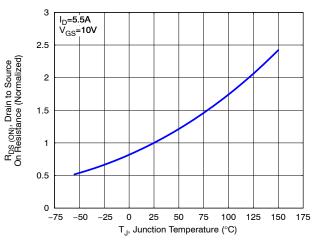


Figure 8. On–Resistance Variation vs.
Temperature

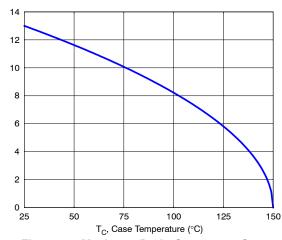


Figure 10. Maximum Drain Current vs. Case Temperature

TYPICAL CHARACTERISTICS

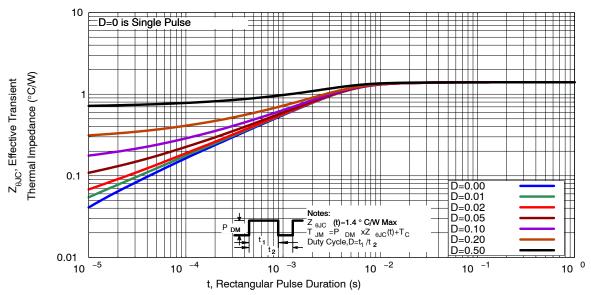
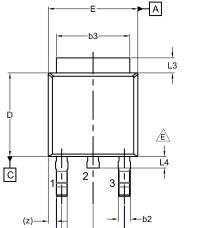


Figure 12. Transient Thermal Impedance

PACKAGE DIMENSIONS

DPAK3 (TO-252 3 LD)

CASE 369AS **ISSUE A**



⊕ 0.25 M AM C

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M-2009.

 D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- F) DIMENSIONS ARE EXCLUSIVE OF BURRS,
- MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

DIM

Α

A1

b

е

e1

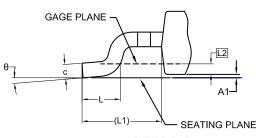
Н

Т

L1

L2

L3



b2 0.76 0.95 1.14 b3 5.34 5.46 5.21 0.45 0.53 0.61 c2 0.45 0.52 0.58 D 5.97 6.10 6.22 D1 5.21 6.35 6.54 6.73 E1 4.32

1 40

2.18

0.00

0.64

MILLIMETERS

2.39

0.127

0.89

1.78

1.27

MIN. NOM. MAX.

2.29

0.77

2.286 BSC

4.572 BSC

9.40 9.91 10.41

1.59

2.90 REF

0.51 BSC

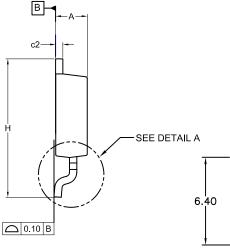
0.89 1.08

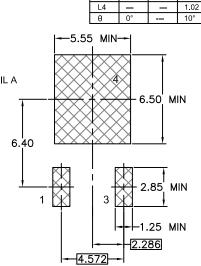
DETAIL A (ROTATED -90°

SCALE: 12X

NON-DIODE PRODUCTS VERSION		
SEE NOTE D 4		
	D1	ĺ
3 2 1 NON-DIODE PRODUCTS VERSION		-

e1





LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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