ANALOG DEVICES

Reinforced, Fast, Low-Power, Six-Channel Digital Isolators

MAX22163–MAX22166

Product Highlights

- **AEC-Q100 Qualification for /V Devices**
- Reinforced Galvanic Isolation for Digital Signals
  - 16-QSOP with 4mm Creepage and Clearance
  - Withstands $3kV_{RMS}$ for 60s (V_{ISO})
  - Continuously Withstands $445V_{RMS}$ (V_{IOWM})
  - Withstands ±10kV Surge Between GNDA and GNDB with 1.2/50µs Waveform
  - High CMTI (50kV/µs, typ)
- Low Power Consumption
  - 0.71mW per Channel at 1Mbps with V_{DD} = 1.8V
  - 1.34mW per Channel at 1Mbps with V_{DD} = 3.3V
  - 3.21mW per Channel at 100Mbps with V_{DD} = 1.8V
- Low Propagation Delay and Low Jitter
  - Maximum Data Rate up to 200Mbps
  - Low Propagation Delay 7ns (typ) at V_{DD} = 3.3V
  - Clock Jitter RMS 11.1ps (typ)
- Safety Regulatory Approvals
  - UL According to UL1577
  - cUL According to CSA Bulletin 5A
  - VDE 0884-11 Reinforced Insulation (Pending)

Key Applications

- Automotive
  - Hybrid Electric Vehicle
  - Chargers
  - Battery Management System (BMS)
  - Inverters

The MAX22163−MAX22166 are a family of six-channel, reinforced, fast, low-power digital galvanic isolators using Analog Devices' proprietary process technology. All devices feature reinforced isolation with a withstand voltage rating of $3kV_{RMS}$ for 60 seconds. Both automotive and general-purpose devices are rated for operation at ambient temperature from -40°C to +125°C.

Devices with /V suffix are AEC-Q100 qualified. See the *Ordering Information* for all automotive grade part numbers.

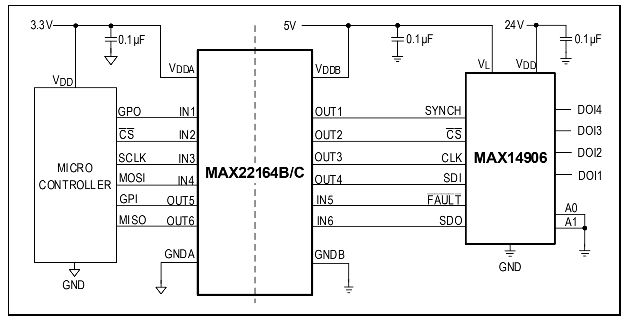
- Industrial
  - Isolated SPI, RS-232/422/485, CAN, Digital I/O
  - Fieldbus Communications
  - Motor Control
  - Medical Systems

These devices transfer digital signals between circuits with different power domains, using as little as 0.71mW per channel at 1Mbps (1.8V supply). The low-power feature reduces system dissipation, increases reliability, and enables compact designs. Devices are available with a maximum data rate of either 25Mbps or 200Mbps and with default-high or default-low outputs. The devices feature low propagation delay and low clock jitter, which reduces system latency.

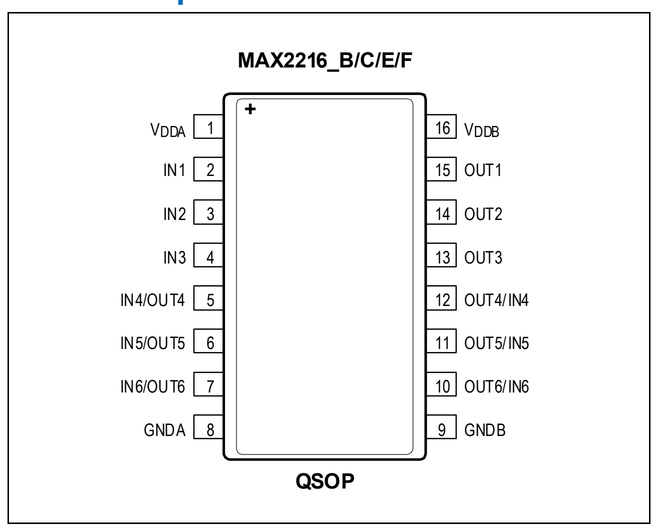
Independent 1.71V to 5.5V supplies on each side also make the devices suitable for use as level translators.

The MAX22163 features three channels transmitting digital signals in one direction and three in opposite; the MAX22164 offers four channels transmitting digital signals in one direction and two in opposite; the MAX22165 provides five channels transmitting digital signals in one direction and one in opposite; the MAX22166 features all six channels transmitting digital signals in one direction.

Simplified Application Diagram



Pin Description



***Ordering Information* appears at end of data sheet.**

19-101240; Rev 6; 11/23

Absolute Maximum Ratings

V_{DDA} to GNDA .... -0.3V to +6V
V_{DDB} to GNDB .... -0.3V to +6V
IN_ on Side A, ENA, DEFA to GNDA .... -0.3V to +6V
IN_ on Side B, ENB, DEFB to GNDB .... -0.3V to +6V
OUT_ on Side A to GNDA ....-0.3V to (V_{DDA} + 0.3V)
OUT_ on Side B to GNDB ....-0.3V to (V_{DDB} + 0.3V)
Short-Circuit Continuous Current
OUT_ on Side A to GNDA .... ±30mA
OUT_ on Side B to GNDB .... ±30mA
Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 8.98mW/°C above +70°C)........... 718.78mW
Temperature Ratings
Operating Temperature Range.................. -40°C to +125°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range..................... -60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow)................................+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 16 QSOP	
Package Code	E16MS+2
Outline Number	21-0055
Land Pattern Number	90-0167
THERMAL RESISTANCE, FOUR LAYER BOARD:	
Junction-to-Ambient (θ_{JA})	111.30°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	57.50°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

DC Electrical Characteristics

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE							
Supply Voltage	V_{DDA}	Relative to GNDA		1.71		5.5	V
	V_{DDB}	Relative to GNDB		1.71		5.5	
Undervoltage-Lockout Threshold	$V_{UVLO\_}$	V_{DD} rising		1.5	1.6	1.66	V
Undervoltage-Lockout Threshold Hysteresis	V_{UVLO_HYST}				45		mV
MAX22163 SUPPLY CURRENT (Note 2)							
Side A Supply Current	I_{DDA}	500kHz square wave, C_L = 0pF	V_{DDA} = 5V		1.23	2.28	mA
			V_{DDA} = 3.3V		1.22	2.25	
			V_{DDA} = 2.5V		1.21	2.24	
			V_{DDA} = 1.8V		1.18	1.97	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		7.83	10.26	
			V_{DDA} = 3.3V		6.47	8.71	
			V_{DDA} = 2.5V		5.90	8.03	
			V_{DDA} = 1.8V		5.35	7.10	
Side B Supply Current	I_{DDB}	500kHz square wave, C_L = 0pF	V_{DDB} = 5V		1.23	2.28	mA
			V_{DDB} = 3.3V		1.22	2.25	
			V_{DDB} = 2.5V		1.21	2.24	
			V_{DDB} = 1.8V		1.18	1.97	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		7.83	10.26	
			V_{DDB} = 3.3V		6.47	8.71	
			V_{DDB} = 2.5V		5.90	8.03	
			V_{DDB} = 1.8V		5.35	7.10	
MAX22164 SUPPLY CURRENT (Note 2)							
Side A Supply Current	I_{DDA}	500kHz square wave, C_L = 0pF	V_{DDA} = 5V		1.09	2.01	mA
			V_{DDA} = 3.3V		1.07	1.99	
			V_{DDA} = 2.5V		1.06	1.98	
			V_{DDA} = 1.8V		1.04	1.66	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		7.63	10.10	
			V_{DDA} = 3.3V		6.67	9.01	
			V_{DDA} = 2.5V		6.28	8.52	
			V_{DDA} = 1.8V		5.84	7.67	
Side B Supply Current	I_{DDB}	500kHz square wave, C_L = 0pF	V_{DDB} = 5V		1.38	2.55	mA
			V_{DDB} = 3.3V		1.36	2.52	
			V_{DDB} = 2.5V		1.35	2.51	
			V_{DDB} = 1.8V		1.32	2.28	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		8.04	10.38	
			V_{DDB} = 3.3V		6.27	8.41	

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			V_{DDB} = 2.5V		5.54	7.53	
			V_{DDB} = 1.8V		4.87	6.53	
MAX22165 SUPPLY CURRENT (Note 2)							
Side A Supply Current	I_{DDA}	500kHz square wave, C_L = 0pF	V_{DDA} = 5V		0.94	1.74	mA
			V_{DDA} = 3.3V		0.93	1.72	
			V_{DDA} = 2.5V		0.92	1.71	
			V_{DDA} = 1.8V		0.90	1.34	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		7.44	9.96	
			V_{DDA} = 3.3V		6.88	9.31	
			V_{DDA} = 2.5V		6.64	9.03	
			V_{DDA} = 1.8V		6.32	8.23	
Side B Supply Current	I_{DDB}	500kHz square wave, C_L = 0pF	V_{DDB} = 5V		1.53	2.82	mA
			V_{DDB} = 3.3V		1.50	2.79	
			V_{DDB} = 2.5V		1.50	2.78	
			V_{DDB} = 1.8V		1.45	2.59	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		8.36	10.64	
			V_{DDB} = 3.3V		6.16	8.19	
			V_{DDB} = 2.5V		5.24	7.10	
			V_{DDB} = 1.8V		4.45	6.01	
MAX22166 SUPPLY CURRENT (Note 2)							
Side A Supply Current	I_{DDA}	500kHz square wave, C_L = 0pF	V_{DDA} = 5V		0.79	1.47	mA
			V_{DDA} = 3.3V		0.78	1.45	
			V_{DDA} = 2.5V		0.78	1.44	
			V_{DDA} = 1.8V		0.75	1.02	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		7.25	9.81	
			V_{DDA} = 3.3V		7.08	9.61	
			V_{DDA} = 2.5V		7.00	9.52	
			V_{DDA} = 1.8V		6.78	8.79	
Side B Supply Current	I_{DDB}	500kHz square wave, C_L = 0pF	V_{DDB} = 5V		1.67	3.09	mA
			V_{DDB} = 3.3V		1.65	3.06	
			V_{DDB} = 2.5V		1.64	3.05	
			V_{DDB} = 1.8V		1.59	2.89	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		8.57	10.81	
			V_{DDB} = 3.3V		5.97	7.91	
			V_{DDB} = 2.5V		4.89	6.62	
			V_{DDB} = 1.8V		3.97	5.44	
LOGIC INTERFACE (IN_, OUT_)							
Input High Voltage	V_{IH}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V		0.7 x $V_{DD\_}$			V

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		1.71V ≤ $V_{DD\_}$ < 2.25V	0.75 x $V_{DD\_}$			
Input Low Voltage	V_{IL}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V			0.8	V
		1.71V ≤ $V_{DD\_}$ < 2.25V			0.7	
Input Hysteresis	V_{HYS}	MAX2216_B/E		410		mV
		MAX2216_C/F		80		
Input Pullup Current	I_{PU}	MAX2216_B/C	-10	-5	-1.5	μA
Input Pulldown Current	I_{PD}	MAX2216_E/F	1.5	5	10	μA
Input Capacitance	C_{IN}	f_{SW} = 1MHz		2		pF
Output Voltage High	V_{OH}	I_{OUT} = -4mA source	$V_{DD\_}$ - 0.4			V
Output Voltage Low	V_{OL}	I_{OUT} = 4mA sink			0.4	V

Dynamic Characteristics - MAX2216_C/F

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	IN_ = GND_ or $V_{DD\_}$ (Note 5)			50		kV/μs
Maximum Data Rate	DR_{MAX}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V		200			Mbps
		1.71V ≤ $V_{DD\_}$ < 2.25V		150			
Minimum Pulse Width	PW_{MIN}	IN_ to OUT_	2.25V ≤ $V_{DD\_}$ ≤ 5.5V			5	ns
			1.71V ≤ $V_{DD\_}$ < 2.25V			6.67	
Propagation Delay (*Figure 1*)	t_{PLH}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	4.4	6.2	9.5	ns
Propagation Delay (*Figure 1*)	t_{PLH}	IN_ to OUT_, C_L = 15pF	3.0V ≤ $V_{DD\_}$ ≤ 3.6V	4.8	7.0	11.2	ns
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	5.3	8.3	14.7	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	7.1	12.3	22.1	
	t_{PHL}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	4.6	6.5	9.9	
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	5.0	7.3	11.6	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	5.4	8.5	14.9	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	7.2	12.1	21.8	
Pulse Width Distortion	PWD	$\|t_{PLH} - t_{PHL}\|$	4.5V ≤ $V_{DD\_}$ ≤ 5.5V		0.4	2.0	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V		0.4	2.0	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V		0.3	2.0	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V		0	2.0	
	t_{SPLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				3.7	ns

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay Skew Part-to-Part (Same Channel)		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				4.7	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				6.9	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				12.1	
	t_{SPHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				4.0	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				4.9	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				7.0	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				11.8	
Propagation Delay Skew Channel-to-Channel (Same Direction) (*Figure 1*)	t_{SCSLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				2.0	ns
	t_{SCSHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				2.0	
Propagation Delay Skew Channel-to-Channel (Opposite Direction)	t_{SCOLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				3.7	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				4.7	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				6.9	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				12.1	
	t_{SCOHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				4.0	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				4.9	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				7.0	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				11.8	
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	200Mbps			100		ps
Clock Jitter RMS	$t_{JCLK(RMS)}$	500kHz clock input, rising/falling edges			11.1		ps
Rise Time (*Figure 1*)	t_R	C_L = 5pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			0.8	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			1.1	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			1.5	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			2.4	
Fall Time (*Figure 1*)	t_F	C_L = 5pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			1.0	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			1.4	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			1.9	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			3.0	

Dynamic Characteristics - MAX2216_B/E

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} – V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	IN_ = GND_ or $V_{DD\_}$ (Note 5)		50		kV/µs
Maximum Data Rate	DR_{MAX}		25			Mbps
Minimum Pulse Width	PW_{MIN}	IN_ to OUT_			40	ns
Glitch Rejection		IN_ to OUT_	10	17	29	ns

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} – V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay (Figure 1)	t_{PLH}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	16.7	22.6	30.7	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	17.0	23.4	32.2	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	17.7	24.8	35.3	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	19.6	28.8	42.8	
	t_{PHL}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	16.4	22.7	32.1	
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	16.8	23.5	33.8	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	17.3	24.8	36.7	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	19.0	28.4	43.7	
Pulse Width Distortion	PWD	$\|t_{PLH} - t_{PHL}\|$	4.5V ≤ $V_{DD\_}$ ≤ 5.5V		0.2	4.0	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V		0.2	4.0	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V		0.3	4.0	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V		0.6	4.0	
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				14.0	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				13.8	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				15.2	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				21.9	
	t_{SPHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				13.0	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				13.5	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				15.4	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				21.4	
Propagation Delay Skew Channel-to-Channel (Same Direction) (Figure 1)	t_{SCSLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				4.0	ns
	t_{SCSHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				4.0	
Propagation Delay Skew Channel-to-Channel (Opposite Direction)	t_{SCOLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				14.0	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				13.8	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				15.2	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				21.9	
	t_{SCOHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				13.0	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				13.5	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				15.4	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				21.4	
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	25Mbps			250		ps
Rise Time (Figure 1)	t_R	C_L = 5pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			0.8	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			1.1	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			1.5	

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} – V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			2.4	
Fall Time (*Figure 1*)	t_F	C_L = 5pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			1.0	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			1.4	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			1.9	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			3.0	

Note 1: General purpose devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design and characterization. Automotive devices are 100% production tested at T_A = +25°C and T_A = +125°C.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective grounds (GNDA or GNDB), unless otherwise noted.

Note 4: All measurements are taken with V_{DDA} = V_{DDB}, unless otherwise noted.

Note 5: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB (V_{CM} = 1000V).

ESD Protection

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
ESD		Human Body Model, All Pins	±4	kV
		IEC 61000-4-2 Contact, GNDB to GNDA	±6	kV

Test Circuit and Timing Diagram

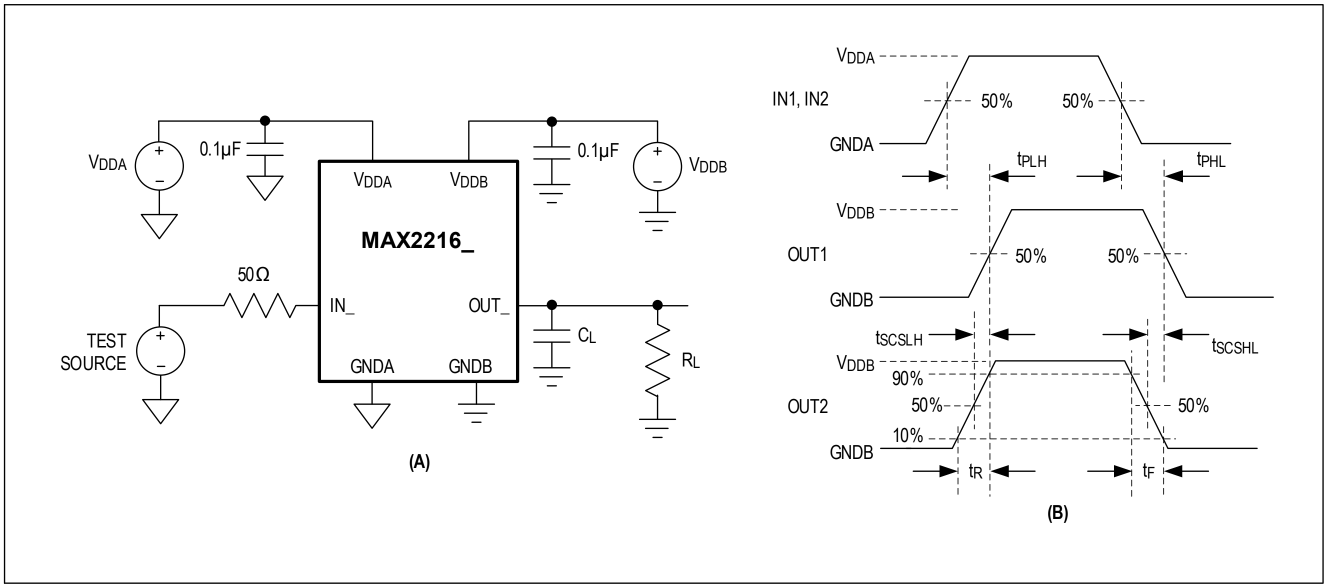


Figure 1. Test Circuit (A) and Timing Diagram (B)

Table 1. Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	1182	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 6)	630	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 6)	445	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (Note 6)	4242	V_P
Maximum Withstanding Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Notes 6, 7)	3000	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Reinforced Insulation, test method per IEC 60065, V_{TEST} = 1.6 x V_{IOSM} = 10,000V_{PEAK} (Notes 6, 9)	6250	V_P
Isolation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500V, T_S = 150°C	$>10^{9}$	
Barrier Capacitance Side A to Side B	C_{IO}	f_{SW} = 1MHz (Note 8)	1.5	pF
Minimum Creepage Distance	CPG		4	mm
Minimum Clearance Distance	CLR		4	mm
Internal Clearance		Distance through insulation	0.021	mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)	>400	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 6: V_{ISO}, V_{IOWM}, V_{IOTM}, V_{IORM}, and V_{IOSM} are defined by the IEC 60747-5-5 standard.
Note 7: Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.
Note 8: Capacitance is measured with all pins on the A and B sides tied together.
Note 9: Devices are immersed in oil during surge characterization.

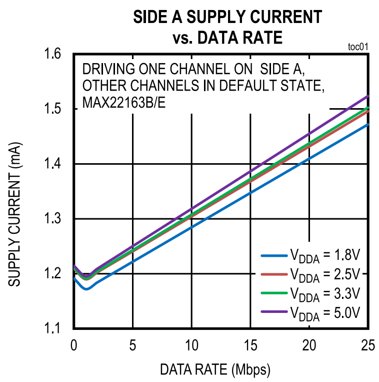
Safety Regulatory Approvals

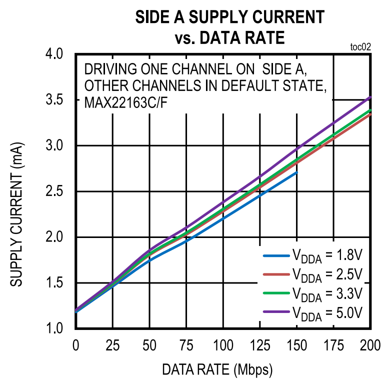
UL
The MAX22163−MAX22166 are certified under UL1577. For more details, refer to file E351759.
Rated up to 3000V_{RMS} isolation voltage for single protection.
cUL (Equivalent to CSA notice 5A)
The MAX22163−MAX22166 are certified up to 3000V_{RMS} for single protection. For more details, refer to file E351759.
VDE (Pending)
The MAX22163−MAX22166 are certified to DIN VDE V 0884-11: 2017-1. Reinforced Insulation, Maximum Transient Isolation Voltage 4242V_{PK}, Maximum Repetitive Peak Isolation Voltage 630V_{PK}.

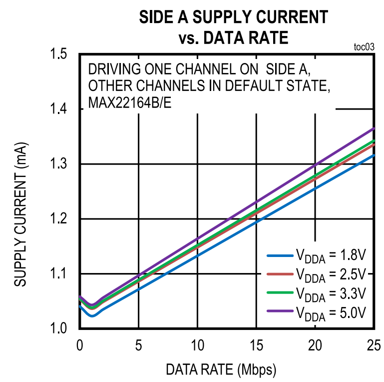
These couplers are suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

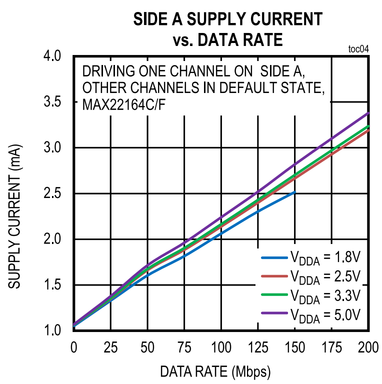
Typical Operating Characteristics

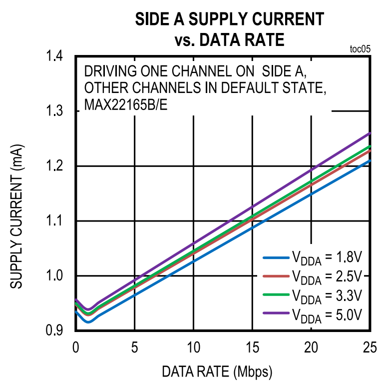
(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

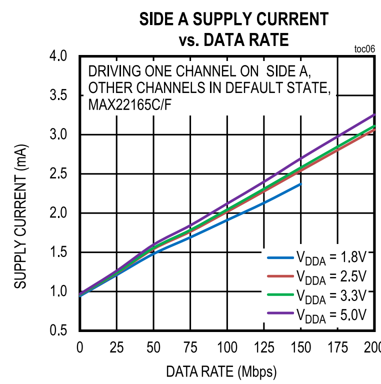


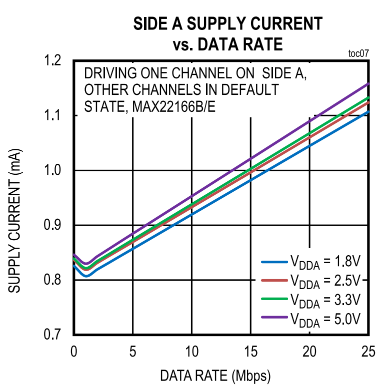


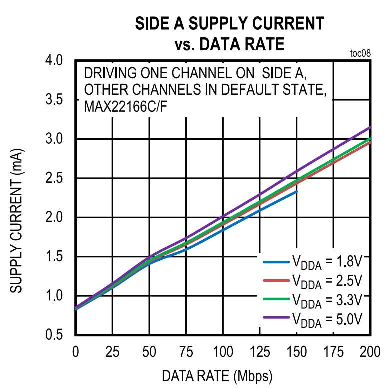


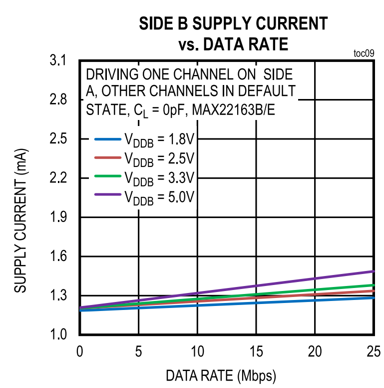




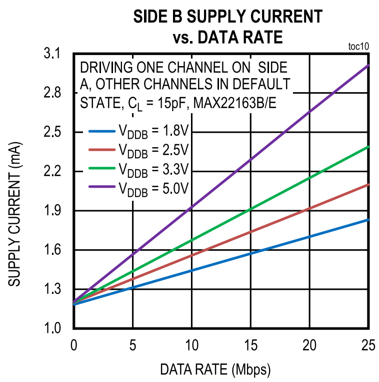


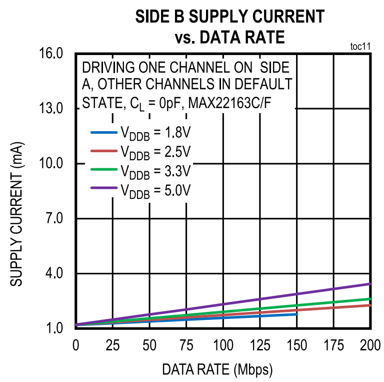


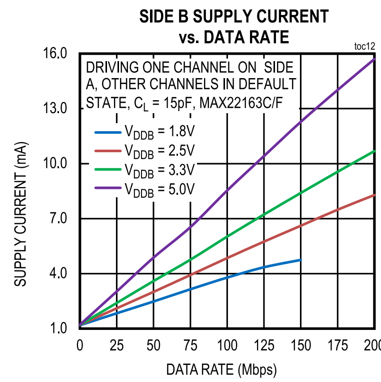


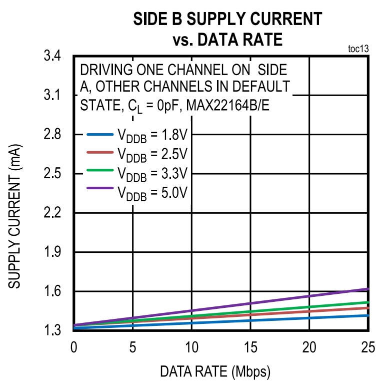


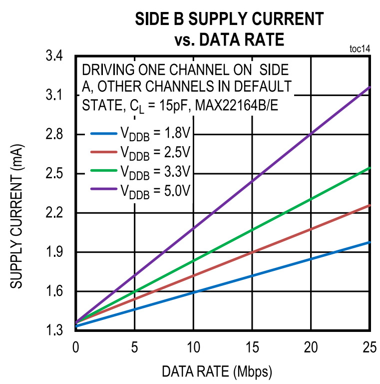
(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

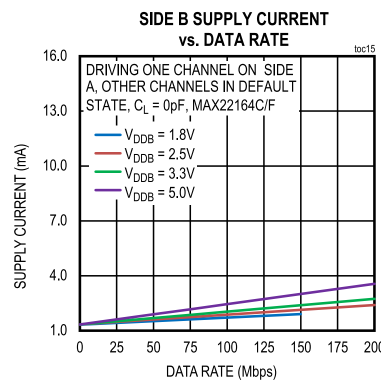


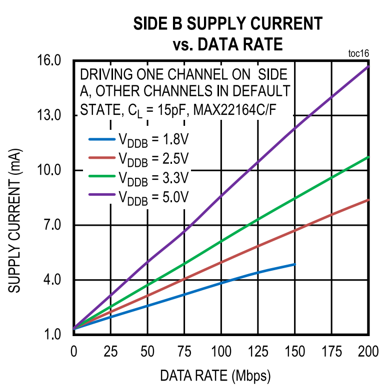


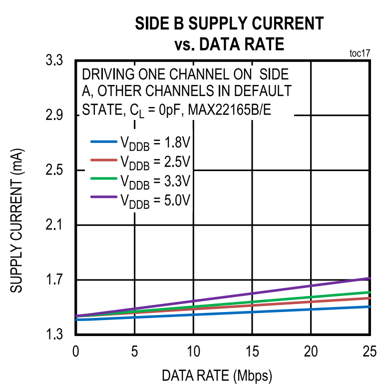


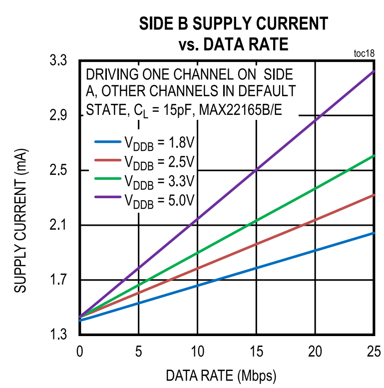




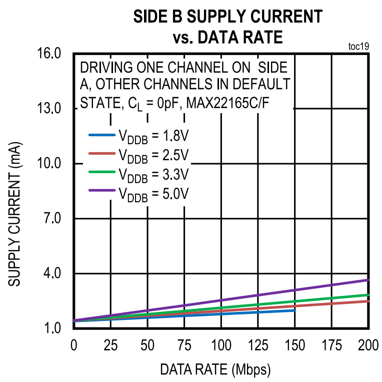


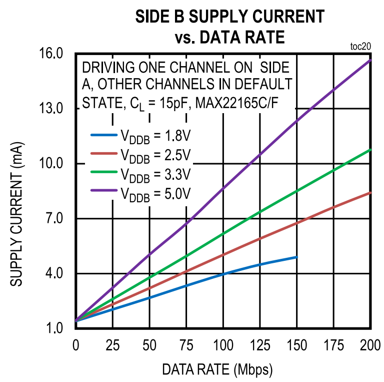


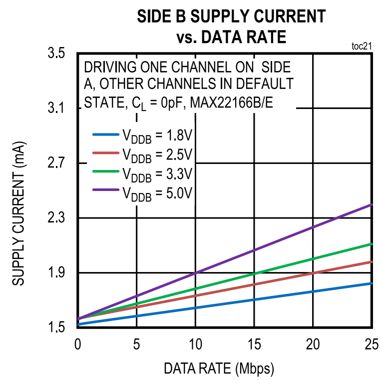


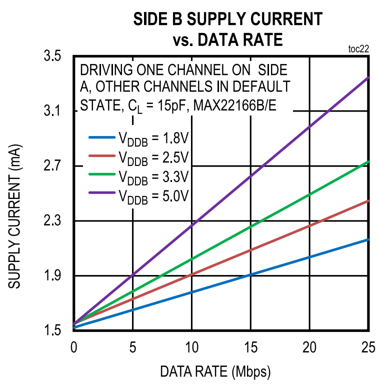


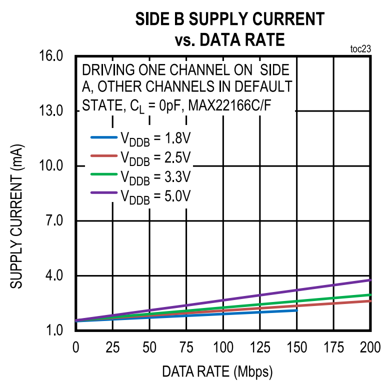
(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

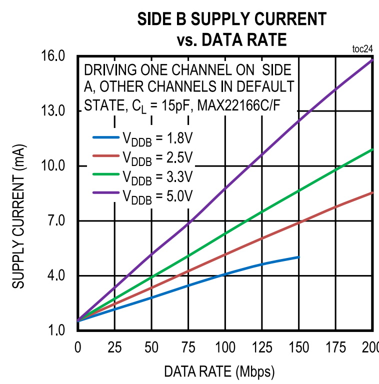


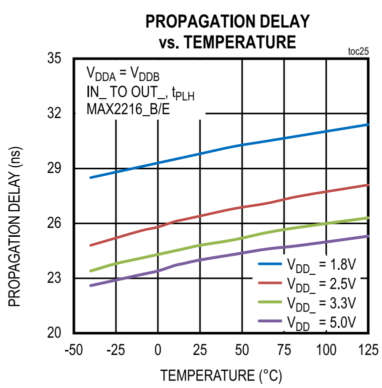


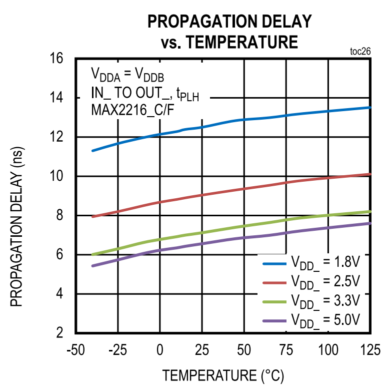


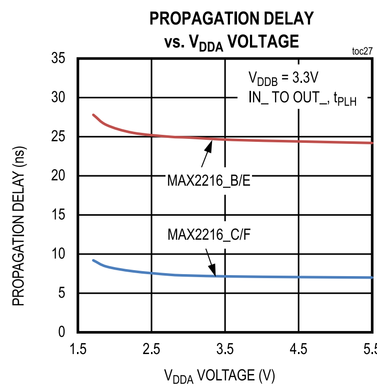












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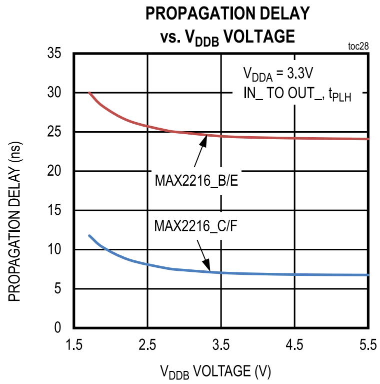
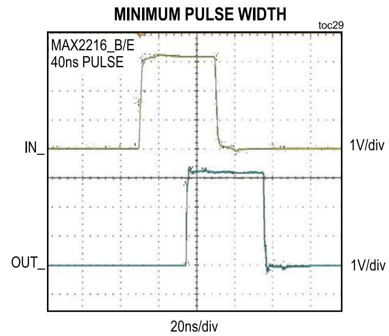
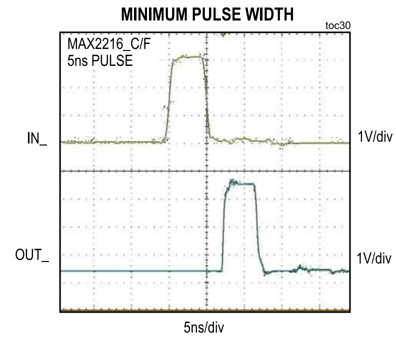
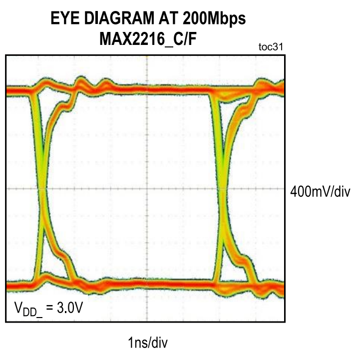
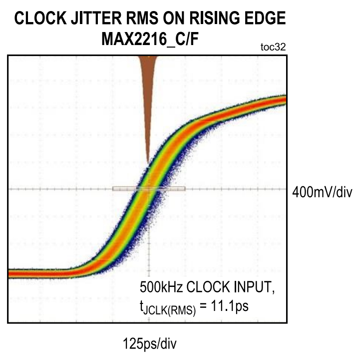
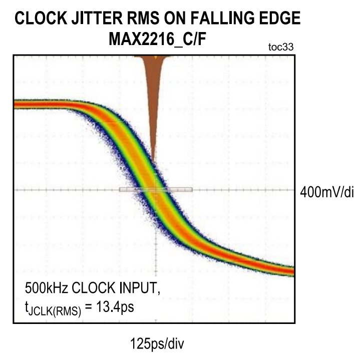


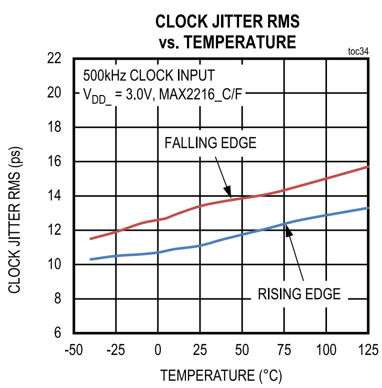




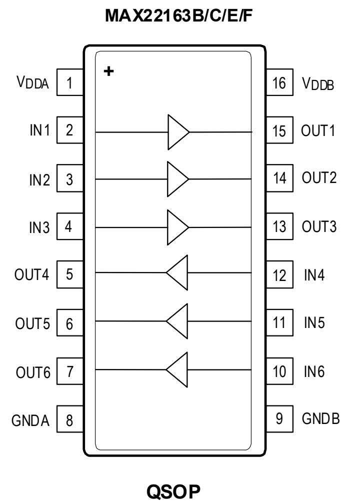


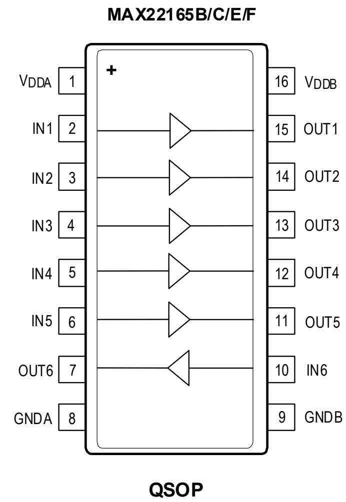


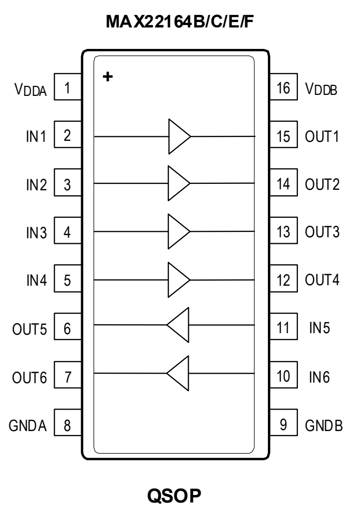


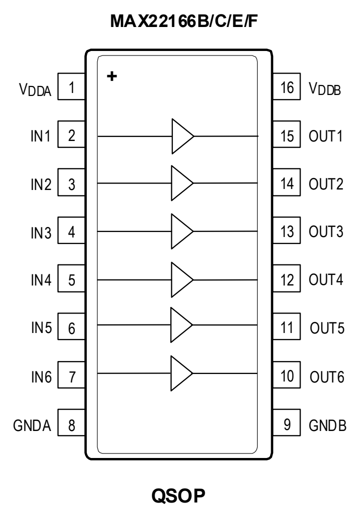


Pin Configurations





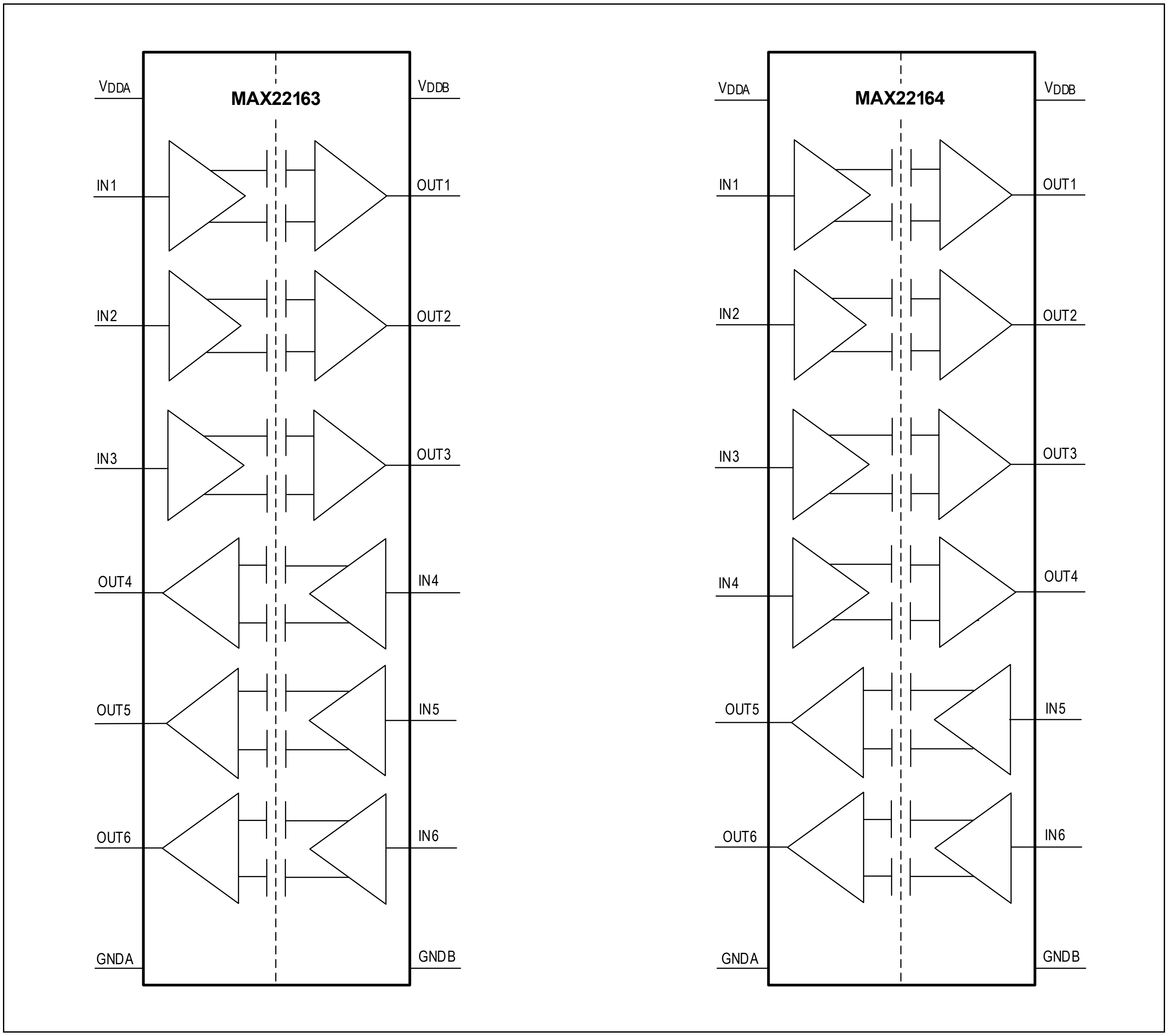


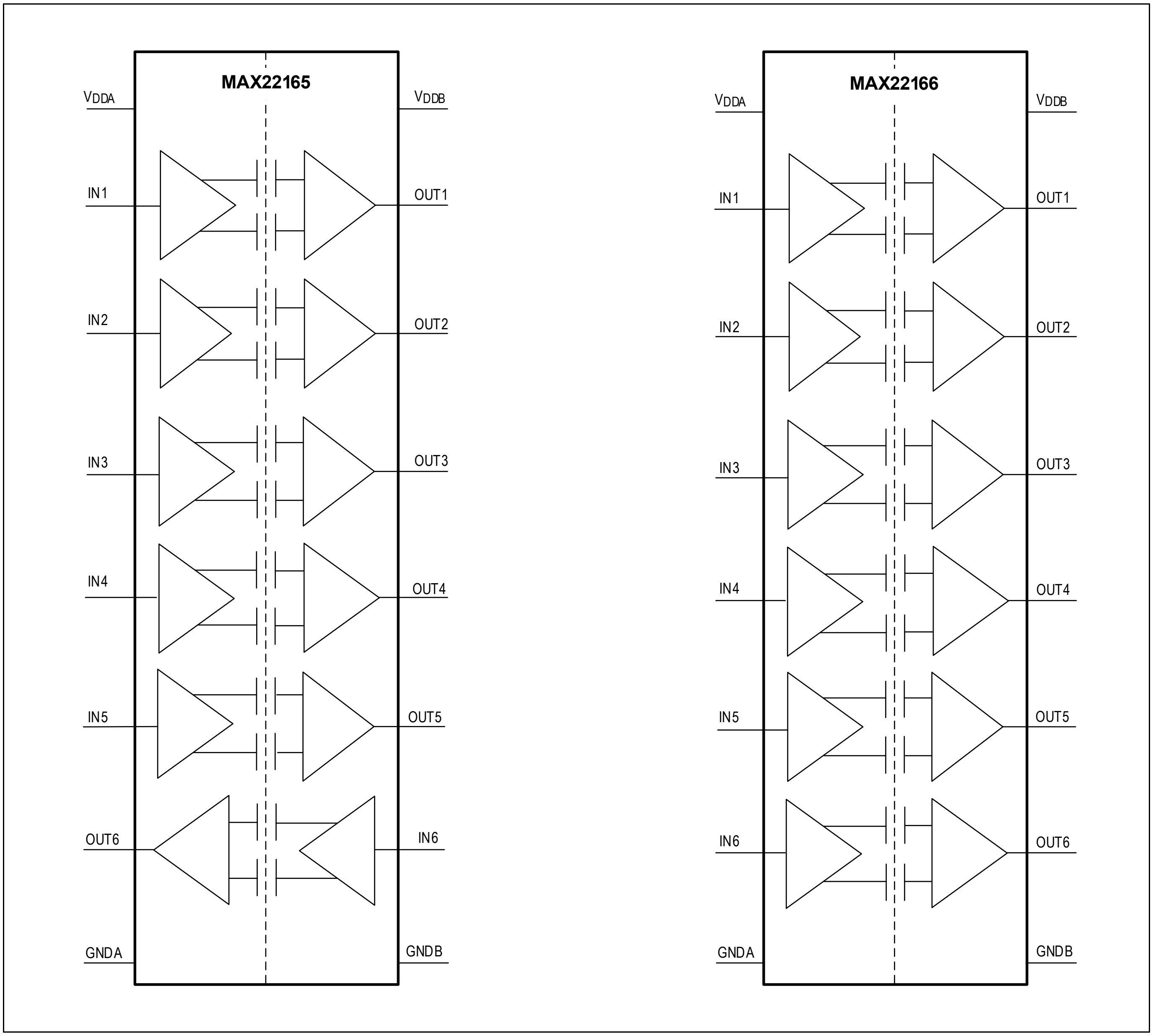


Pin Descriptions

PIN				NAME	FUNCTION
MAX22163	MAX22164	MAX22165	MAX22166		
1	1	1	1	V_{DDA}	Power Supply Input for Side A. Bypass V_{DDA} to GNDA with a 0.1µF ceramic capacitor as close as possible to the pin.
2	2	2	2	IN1	Logic Input 1 on Side A. Corresponds to Logic Output 1 on Side B.
3	3	3	3	IN2	Logic Input 2 on Side A. Corresponds to Logic Output 2 on Side B.
4	4	4	4	IN3	Logic Input 3 on Side A. Corresponds to Logic Output 3 on Side B.
12	5	5	5	IN4	Logic Input 4 on Side A/B. Corresponds to Logic Output 4 on Side B/A.
11	11	6	6	IN5	Logic Input 5 on Side A/B. Corresponds to Logic Output 5 on Side B/A.
10	10	10	7	IN6	Logic Input 6 on Side A/B. Corresponds to Logic Output 6 on Side B/A.
8	8	8	8	GNDA	Ground Reference for Side A.
9	9	9	9	GNDB	Ground Reference for Side B.
7	7	7	10	OUT6	Logic Output 6 on Side B/A. OUT6 is the logic output for the IN6 input on Side A/B.
6	6	11	11	OUT5	Logic Output 5 on Side B/A. OUT5 is the logic output for the IN5 input on Side A/B.
5	12	12	12	OUT4	Logic Output 4 on Side B/A. OUT4 is the logic output for the IN4 input on Side A/B.
13	13	13	13	OUT3	Logic Output 3 on Side B. OUT3 is the logic output for the IN3 input on Side A.
14	14	14	14	OUT2	Logic Output 2 on Side B. OUT2 is the logic output for the IN2 input on Side A.
15	15	15	15	OUT1	Logic Output 1 on Side B. OUT1 is the logic output for the IN1 input on Side A.
16	16	16	16	V_{DDB}	Power Supply Input for Side B. Bypass V_{DDB} to GNDB with a 0.1µF ceramic capacitor as close as possible to the pin.

Functional Diagrams




MAX22165
VDDA
VDDB
IN1
OUT1
IN2
OUT2
IN3
OUT3
IN4
OUT4
IN5
OUT5
OUT6
IN6
GNDA
GNDB
MAX22166
VDDA
VDDB
IN1
OUT1
IN2
OUT2
IN3
OUT3
IN4
OUT4
IN5
OUT5
IN6
OUT6
GNDA
GNDB

Detailed Description

The MAX22163−MAX22166 are a family of six-channel reinforced digital isolators in a 16-QSOP package, with an isolation rating of 3kV$_{RMS}$. This family of devices offers all possible unidirectional channel configurations to accommodate any six-channel design.

The MAX22163 features three channels transmitting digital signals in one direction and three channels transmitting in the opposite direction for applications such as isolated microcontroller interfaces. The MAX22164 offers four channels transmitting digital signals in one direction and two channels transmitting in the opposite direction, making them ideal for applications such as isolated SPI. The MAX22165 provides five channels transmitting digital signals in one direction and one channel transmitting in the opposite direction. The MAX22166 features all six channels transmitting digital signals in one direction, which are suitable in applications such as isolated digital I/O.

The MAX22163−MAX22166 are available in a 16-pin QSOP package with 4mm creepage and clearance, with an isolation rating of 3kV$_{RMS}$. This family of digital isolators offers low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Analog Devices' proprietary process technology. The devices isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry.

Devices are available with a maximum data rate of either 25Mbps (B/E version) or 200Mbps (C/F version). The MAX2216_B/C feature default-high outputs. The MAX2216_E/F feature default-low outputs. The output assumes the default state when the input is not powered or if the input is open-circuit. The MAX22163-MAX22166 have two supply inputs (V_{DDA} and V_{DDB}) that independently set the logic levels on either side of the device. V_{DDA} and V_{DDB} are referenced to GNDA and GNDB, respectively. The MAX22163−MAX22166 also feature a refresh circuit to ensure output accuracy when an input remains in the same state indefinitely.

Digital Isolation

The family of devices provides reinforced galvanic isolation for digital signals transmitted between two ground domains. The MAX22163−MAX22166 can withstand differences of up to 3kV$_{RMS}$ for up to 60 seconds, and up to 630V$_{PEAK}$ of continuous isolation.

AEC-Q100 Qualification

Devices with /V suffix are AEC-Q100 qualified. See the *Ordering Information* table for all automotive grade part numbers.

Level Shifting

The wide supply voltage range of both V_{DDA} and V_{DDB} allows the MAX22163−MAX22166 to be used for level translation in addition to isolation. V_{DDA} and V_{DDB} can be independently set to any voltage from 1.71V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Unidirectional Channels

Each channel of the device is unidirectional; it only passes data in one direction, as indicated in the *Functional Diagrams*. All devices feature six unidirectional channels that operate independently with guaranteed data rates from DC to 25Mbps (B/E version), or from DC to 200Mbps (C/F version). The output driver of each channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Startup and Undervoltage Lockout

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or normal operation due to a sagging supply voltage. When an undervoltage condition is detected on either supply, all outputs go to their default states regardless of the state of the inputs, as seen in *Table 2*. *Figure 2* through *Figure 5* show the behavior of the outputs during power-up and power-down.

Table 2. Output Behavior During Undervoltage Conditions

$V_{IN\_}$	V_{DDA}	V_{DDB}	V_{OUTA}	V_{OUTB}
1	Powered	Powered	High	High
0	Powered	Powered	Low	Low
X	Undervoltage	Powered	Default	Default
X	Powered	Undervoltage	Default	Default

Note: 'X' is don't care.

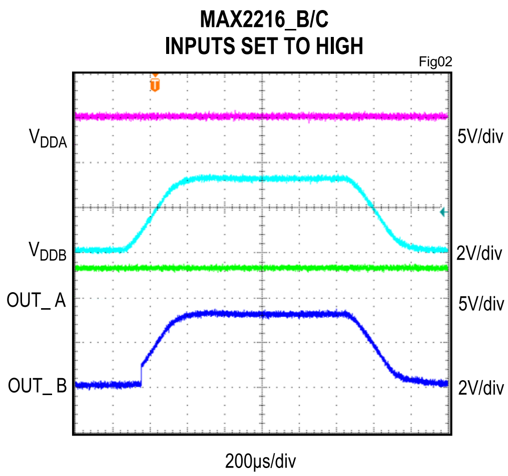


Figure 2. Undervoltage Lockout Behavior, MAX2216_B/C, Inputs Set to High

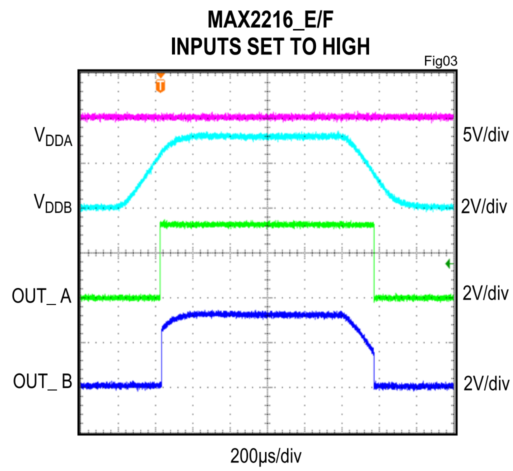


Figure 3. Undervoltage Lockout Behavior, MAX2216_E/F, Inputs Set to High

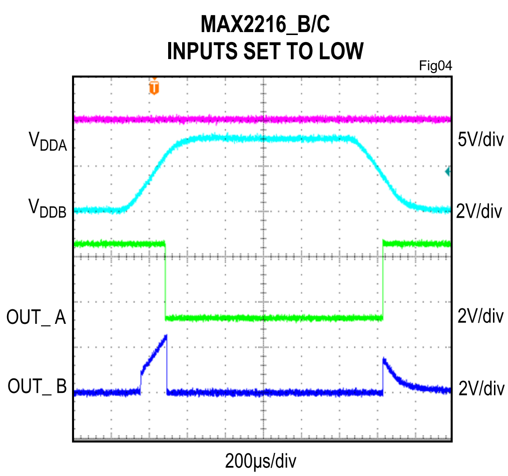


Figure 4. Undervoltage Lockout Behavior, MAX2216_B/C, Inputs Set to Low

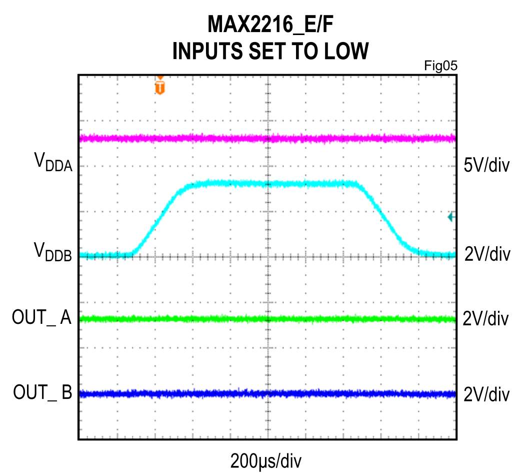


Figure 5. Undervoltage Lockout Behavior, MAX2216_E/F, Inputs Set to Low

Safety Limit

Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the MAX22163−MAX22166 can dissipate excessive amounts of power. Excessive power dissipation can damage the die and thus the isolation barrier, potentially causing downstream issues. Table 3 shows the safety limits for the MAX22163−MAX22166.

The maximum safety temperature (T_S) for the device is the 150°C maximum junction temperature specified in the Absolute Maximum Ratings. The power dissipation (P_D) and junction-to-ambient thermal impedance (θ_{JA}) determine the junction temperature. Thermal impedance values (θ_{JA} and θ_{JC}) are available in the Package Information section and power dissipation calculations are discussed in the Calculating Power Dissipation section. Calculate the junction temperature (T_J) as:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Figure 6 shows the thermal derating curve for safety limiting the power of the devices, and Figure 7 shows the thermal derating curve for safety limiting the current of the devices. Ensure the junction temperature does not exceed 150°C.

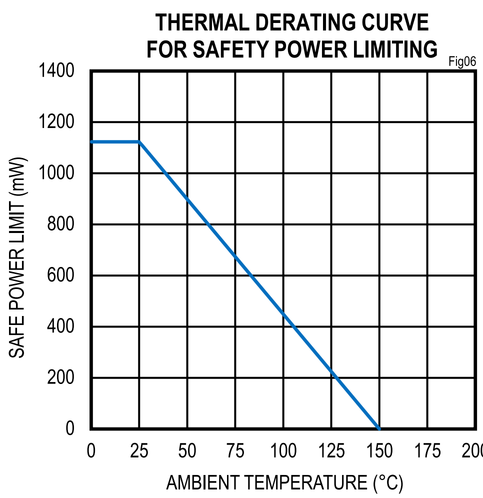


Figure 6. Thermal Derating Curve for Safety Power Limiting

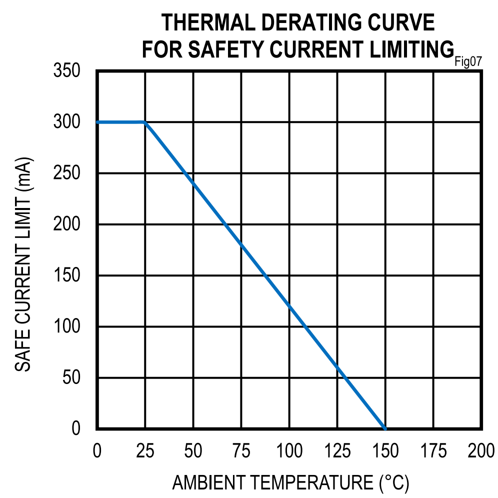


Figure 7. Thermal Derating Curve for Safety Current Limiting

Table 3. Safety Limiting Values

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT
Safety Current on Any Pin (No Damage to Isolation Barrier)	I_S	T_J = 150°C, T_A = 25°C	300	mA
Total Safety Power Dissipation	P_S	T_J = 150°C, T_A = 25°C	1123	mW
Maximum Safety Temperature	T_S		150	°C

Applications Information

Power-Supply Sequencing

The MAX22163−MAX22166 do not require any special power supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1μF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible.

Layout Considerations

The PCB designer should follow some critical recommendations to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low-inductance, avoid using vias.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the devices free from ground and signal planes. Any galvanic or metallic connection between Side A and Side B defeats the isolation.

Calculating Power Dissipation

The required current for a given supply (V_{DDA} or V_{DDB}) can be estimated by summing the current required for each channel. The supply current for a channel depends on if the channel is an input or an output, the channel's data rate, and the capacitive or resistive load if it is an output. The typical current for an input or output at any data rate can be estimated from the graphs in *Figure 8* and *Figure 9*. Note that the data in *Figure 8* and *Figure 9* are extrapolated from the supply current measurements in a typical operating condition.

The total current for a single channel is the sum of the no load current (shown in *Figure 8* and *Figure 9*), which is a function of voltage and data rate, and the load current, which depends on the type of load. Current into a capacitive load is a function of the load capacitance, switching frequency, and supply voltage.

$$I_{CL} = C_L \times f_{SW} \times V_{DD}$$

where:

I_{CL} is the current required to drive the capacitive load.

C_L is the load capacitance on the isolator's output pin.

f_{SW} is the switching frequency (bits per second/2).

V_{DD} is the supply voltage on the output side of the isolator.

Current into a resistive load depends on the load resistance, supply voltage, and average duty cycle of the data waveform. The DC load current can be conservatively estimated by assuming the output is always high.

$$I_{RL} = V_{DD} \div R_L$$

where:

I_{RL} is the current required to drive the resistive load.

V_{DD} is the supply voltage on the output side of the isolator.

R_L is the load resistance on the isolator's output pin.

Example (shown in *Figure 10*): A MAX22164C is operating with V_{DDA} = 2.5V, V_{DDB} = 3.3V, channel 1 operating at 20Mbps with a 15kΩ resistive load; channel 2 operating at 100Mbps with a 10pF capacitive load; channel 3 is not in use and the resistive load is negligible as the isolator is driving a CMOS input; channel 4 held high with a 10kΩ resistive load; channel 5 operating at 50Mbps with a 20kΩ resistive load; and channel 6 operating at 200Mbps with a 15pF capacitive load. See *Table 4* and *Table 5* for V_{DDA} and V_{DDB} supply current calculation worksheets.

V_{DDA} must supply (with V_{DDA} = 2.5V):

- Channel 1 is an input channel operating at 2.5V and 20Mbps, consuming 0.35mA, estimated from *Figure 8*.
- Channel 2 is an input channel operating at 2.5V and 100Mbps, consuming 1.19mA, estimated from *Figure 8*.
- Channels 3 and 4 are input channels operating at 2.5V with DC signal, consuming 0.14mA, estimated from *Figure 8*.
- Channel 5 is an output channel operating at 2.5V and 50Mbps, consuming 0.52mA, estimated from *Figure 9*.
- I_{RL} on channel 5 for 20kΩ resistive load at 2.5V and switching at 50Mbps with 50% duty cycle is 0.0625mA.
- Channel 6 is an output channel operating at 2.5V and 200Mbps, consuming 1.31mA, estimated from *Figure 9*.
- I_{CL} on channel 6 for 15pF capacitive load at 2.5V and 200Mbps is 3.75mA.

Total current for Side A = 7.46mA (typ).

V_{DDB} must supply (with V_{DDB} = 3.3V):

- Channel 1 is an output channel operating at 3.3V and 20Mbps, consuming 0.40mA, estimated from *Figure 9*.
- I_{RL} on channel 1 for 15kΩ resistive load at 3.3V and switching at 20Mbps with 50% duty cycle is 0.11mA.
- Channel 2 is an output channel operating at 3.3V and 100Mbps, consuming 0.96mA, estimated from *Figure 9*.
- I_{CL} on channel 2 for 10pF capacitive load at 3.3V and 100Mbps is 1.65mA.
- Channels 3 and 4 are output channels operating at 3.3V with DC signal, consuming 0.26mA, estimated from *Figure 9*.
- I_{RL} on channel 4 for 10kΩ resistive load held at 3.3V is 0.33mA.
- Channel 5 is an input channel operating at 3.3V and 50Mbps, consuming 0.68mA, estimated from *Figure 8*.
- Channel 6 is an input channel operating at 3.3V and 200Mbps, consuming 2.29mA, estimated from *Figure 8*.

Total current for Side B = 6.94mA (typ).

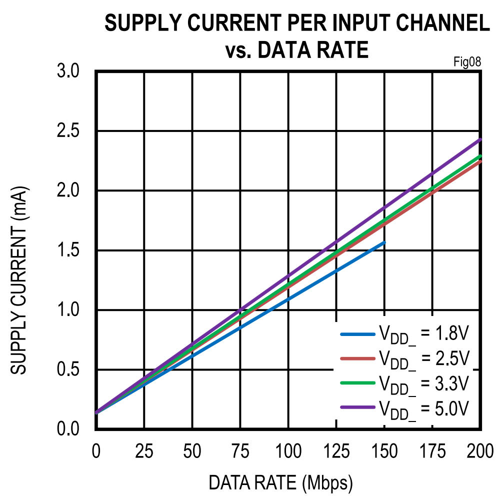


Figure 8. Supply Current Per Input Channel (Calculated)

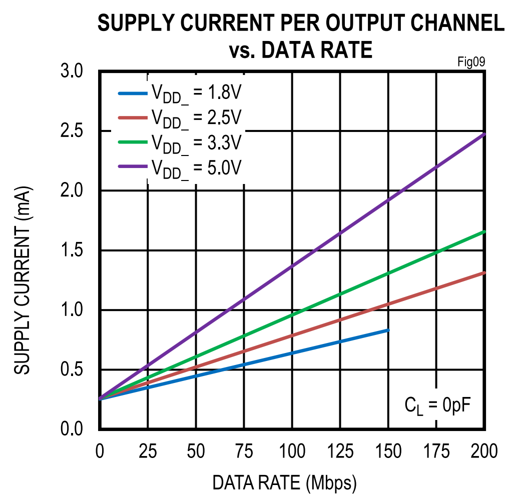


Figure 9. Supply Current Per Output Channel (Calculated)

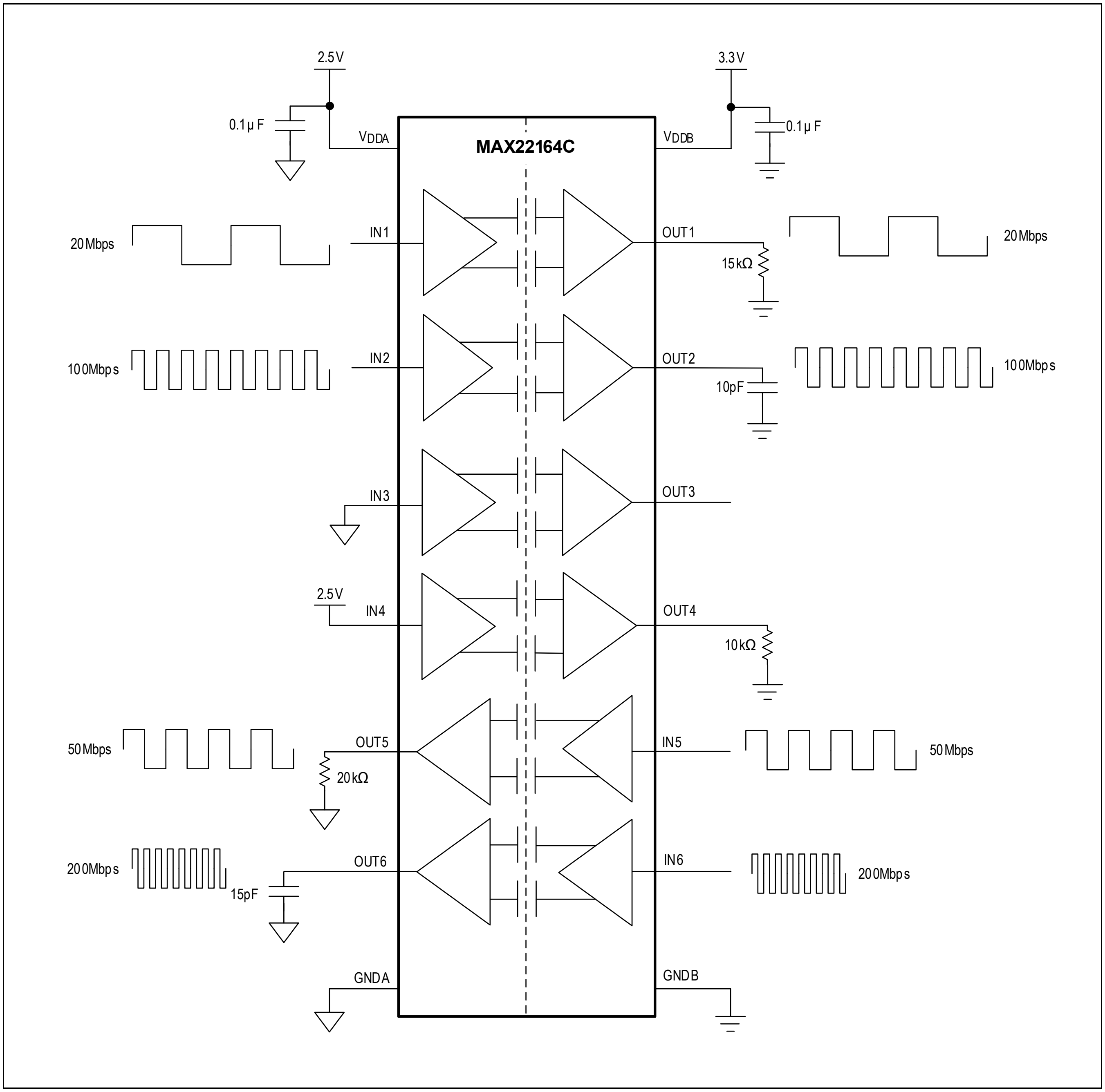


Figure 10. Example Circuit for Supply Current Calculation

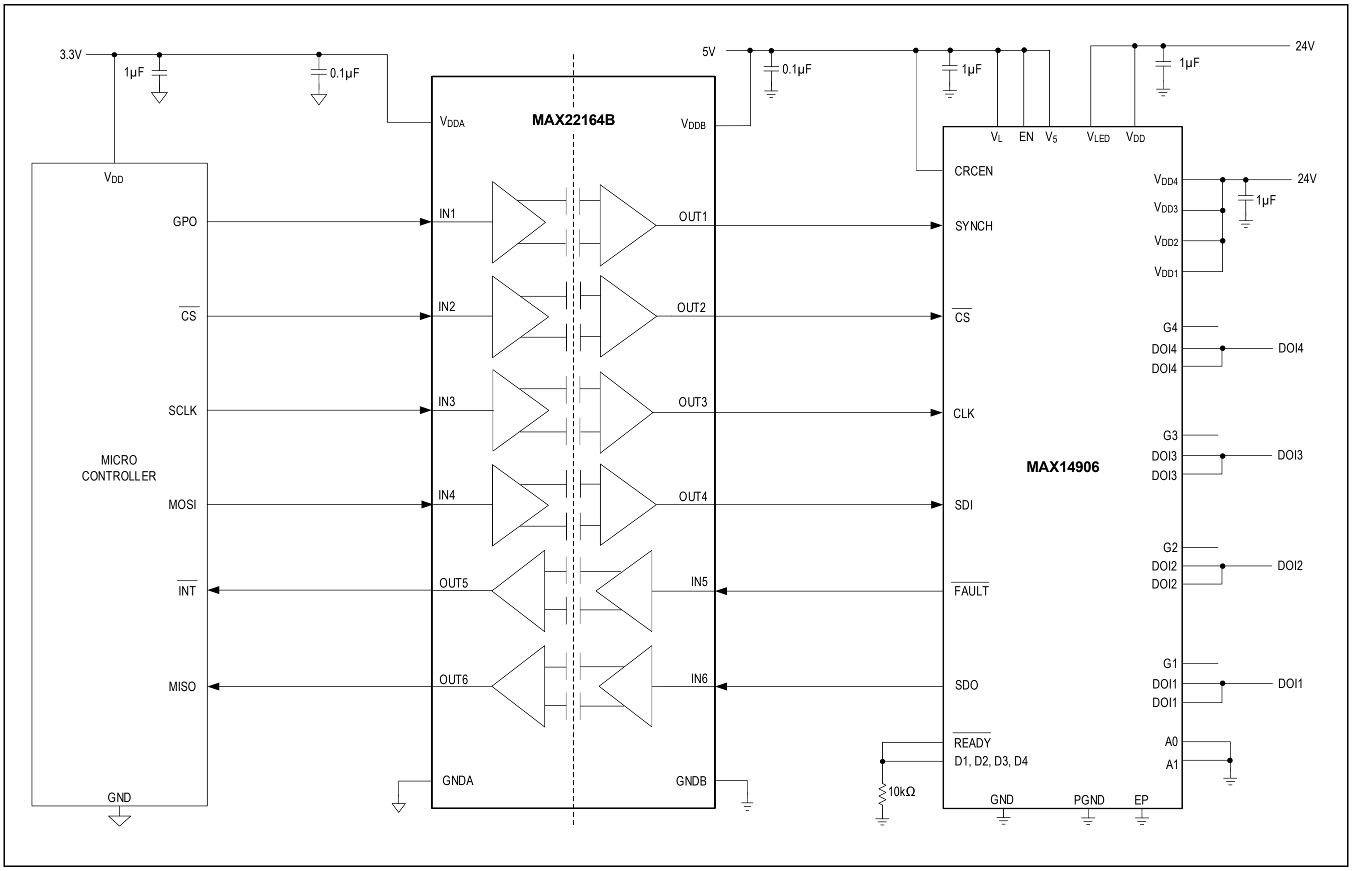
Table 4. Side A Supply Current Calculation Worksheet

SIDE A	V_{DDA} = 2.5V					
CHANNEL	IN/OUT	DATA RATE (Mbps)	LOAD TYPE	LOAD	"NO LOAD" CURRENT (mA)	LOAD CURRENT (mA)
1	IN	20			0.35	
2	IN	100			1.19	
3	IN	0			0.14	
4	IN	0			0.14	
5	OUT	50	Resistive	20kΩ	0.52	2.5V / 20kΩ x 0.5 = 0.0625mA
6	OUT	200	Capacitive	15pF	1.31	2.5V x 100MHz x 15pF = 3.75mA
Total: 7.46mA						

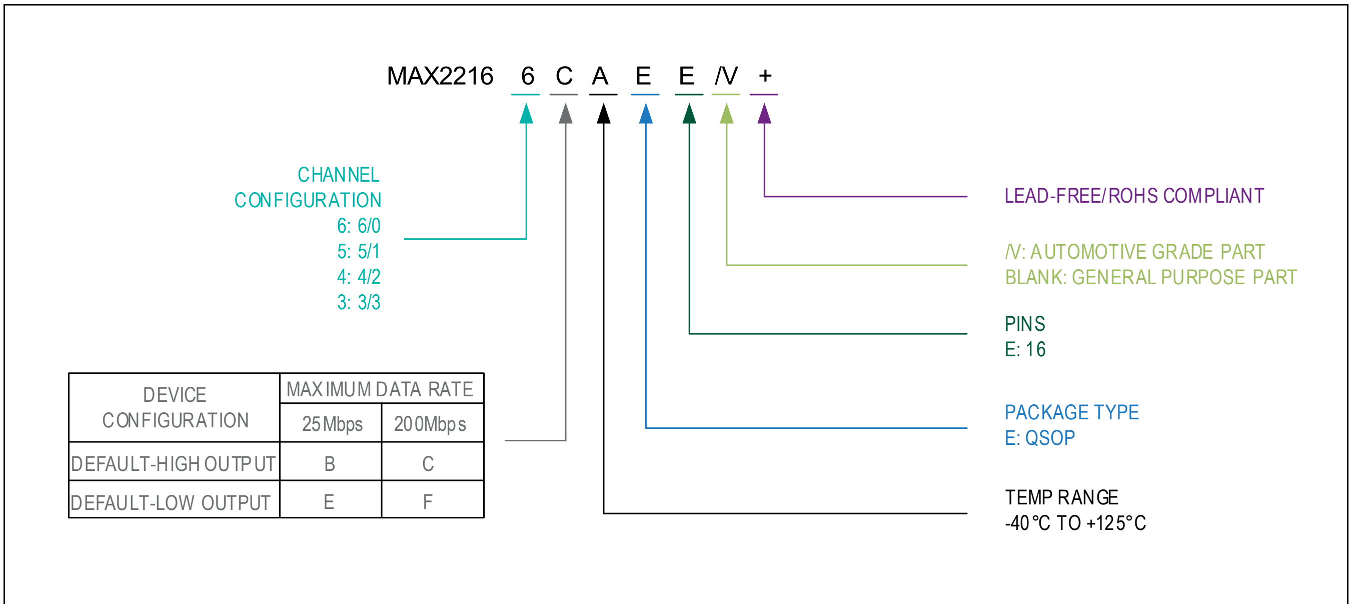
Table 5. Side B Supply Current Calculation Worksheet

SIDE B	V_{DDB} = 3.3V					
CHANNEL	IN/OUT	DATA RATE (Mbps)	LOAD TYPE	LOAD	"NO LOAD" CURRENT (mA)	LOAD CURRENT (mA)
1	OUT	20	Resistive	15kΩ	0.40	3.3V / 15kΩ x 0.5 = 0.11mA
2	OUT	100	Capacitive	10pF	0.96	3.3V x 50MHz x 10pF = 1.65mA
3	OUT	0			0.26	
4	OUT	0	Resistive	10kΩ	0.26	3.3V / 10kΩ = 0.33mA
5	IN	50			0.68	
6	IN	200			2.29	
Total: 6.94mA						

Typical Application Circuits



Product Selector Guide



Ordering Information

PART NUMBER	CHANNEL CONFIGURATION	DATA RATE (Mbps)	DEFAULT OUTPUT	ISOLATION VOLTAGE (kV_{RMS})	TEMPERATURE RANGE (°C)	PIN-PACKAGE
GENERAL PURPOSE DEVICES						
MAX22163BAEE+*	3/3	25	High	3	-40 to +125	16-QSOP
MAX22163CAEE+	3/3	200	High	3	-40 to +125	16-QSOP
MAX22163EAEE+*	3/3	25	Low	3	-40 to +125	16-QSOP
MAX22163FAEE+	3/3	200	Low	3	-40 to +125	16-QSOP
MAX22164BAEE+*	4/2	25	High	3	-40 to +125	16-QSOP
MAX22164CAEE+	4/2	200	High	3	-40 to +125	16-QSOP
MAX22164EAEE+	4/2	25	Low	3	-40 to +125	16-QSOP
MAX22164FAEE+	4/2	200	Low	3	-40 to +125	16-QSOP
MAX22165BAEE+*	5/1	25	High	3	-40 to +125	16-QSOP
MAX22165CAEE+	5/1	200	High	3	-40 to +125	16-QSOP
MAX22165EAEE+*	5/1	25	Low	3	-40 to +125	16-QSOP
MAX22165FAEE+	5/1	200	Low	3	-40 to +125	16-QSOP
MAX22166BAEE+*	6/0	25	High	3	-40 to +125	16-QSOP
MAX22166CAEE+	6/0	200	High	3	-40 to +125	16-QSOP
MAX22166EAEE+*	6/0	25	Low	3	-40 to +125	16-QSOP
MAX22166FAEE+	6/0	200	Low	3	-40 to +125	16-QSOP
AUTOMOTIVE DEVICES						
MAX22163BAEE/V+*	3/3	25	High	3	-40 to +125	16-QSOP
MAX22163CAEE/V+*	3/3	200	High	3	-40 to +125	16-QSOP
MAX22163EAEE/V+*	3/3	25	Low	3	-40 to +125	16-QSOP
MAX22163FAEE/V+	3/3	200	Low	3	-40 to +125	16-QSOP

MAX22164BAEE/V+*	4/2	25	High	3	-40 to +125	16-QSOP
MAX22164CAEE/V+*	4/2	200	High	3	-40 to +125	16-QSOP
MAX22164EAEE/V+*	4/2	25	Low	3	-40 to +125	16-QSOP
MAX22164FAEE/V+*	4/2	200	Low	3	-40 to +125	16-QSOP
MAX22165BAEE/V+*	5/1	25	High	3	-40 to +125	16-QSOP
MAX22165CAEE/V+*	5/1	200	High	3	-40 to +125	16-QSOP
MAX22165EAEE/V+*	5/1	25	Low	3	-40 to +125	16-QSOP
MAX22165FAEE/V+*	5/1	200	Low	3	-40 to +125	16-QSOP
MAX22166BAEE/V+*	6/0	25	High	3	-40 to +125	16-QSOP
MAX22166CAEE/V+*	6/0	200	High	3	-40 to +125	16-QSOP
MAX22166EAEE/V+*	6/0	25	Low	3	-40 to +125	16-QSOP
MAX22166FAEE/V+*	6/0	200	Low	3	-40 to +125	16-QSOP

**Future product − contact Analog Devices for availability.*

+Denotes a lead (Pb)–free/RoHS-compliant package.

/V Denotes an automotive qualified part.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/21	Initial Release	—
1	8/22	Removed future product designation from MAX22164EAEE+ in the *Ordering Information* section	26
2	10/22	Removed future product designation from MAX22163FAEE+ in the *Ordering Information* section	26
3	11/22	Removed future product designation from MAX22164CAEE+ in the *Ordering Information* section	26
4	01/23	Removed future product designation from MAX22164FAEE+ and MAX22165FAEE+ in the *Ordering Information* section	26
5	06/23	Removed future product designation from MAX22163FAEE/V+ in the *Ordering Information* section	26
6	11/23	Removed future product designation from MAX22163CAEE+, MAX22165CAEE+, MAX22166FAEE+ in the *Ordering Information* section	26