Click **here** for production status of specific part numbers.

MAX16972/MAX16972A

3A Automotive Hi-Speed USB Protectors with Apple iPhone/iPad and USB 2.0 Charge Detection

General Description

The MAX16972/MAX16972A provide high-ESD and short-circuit protection for the low-voltage internal USB data and USB power line in automotive radio, navigation, connectivity, and USB hub applications. The devices support both Hi-Speed USB (480Mbps) and full-speed USB (12Mbps) operation. In addition, the devices include integrated circuitry to enable fast charging for consumer devices that adhere to either the Apple® method or the Hi-Speed USB host-charger port-detection protocol and support USB on-the-go (OTG).

The short-circuit protection features include short-to-battery on the protected HVBUS, HVD+, and HVD- outputs, as well as short-to-HVBUS on the protected HVD+ and HVD- outputs. The devices are capable of a short-to-battery condition of up to +18V. Short-to-GND and overcurrent protection are also provided on the HVBUS output to protect the internal BUS power rail from overcurrent faults.

Each device features high-ESD protection to ±15kV Air-Gap method and ±8kV Contact method on all protected HVBUS, HVD+, and HVD- outputs.

Each device features two low 4.0Ω on-resistance Hi-Speed USB switches, a current-limited low-voltage 31mΩ BUS switch, and provides an integrated high-voltage external power-switch controller. The BUS switch can start up into high-capacitance noncompliant USB loads. The devices also feature an enable input, a fault output, integrated Apple iPhone®/iPad® fast-charging termination resistors, and an integrated host-charger port-detection circuit that adheres to the USB 2.0 battery-charging specification version 1.2.

The devices are available in 16-pin QSOP and 16-pin (4mm x 4mm) TQFN packages, and operate over the -40°C to +105°C temperature range. The MAX16972 and MAX16972A are drop-in compatible with the MAX16970, MAX16971, MAX16970A, MAX16971A, MAX16917, MAX16919, and MAX16969 devices.

Applications

- Automotive Radio and Navigation
- USB Hub
- Automotive Connectivity
- Telematics

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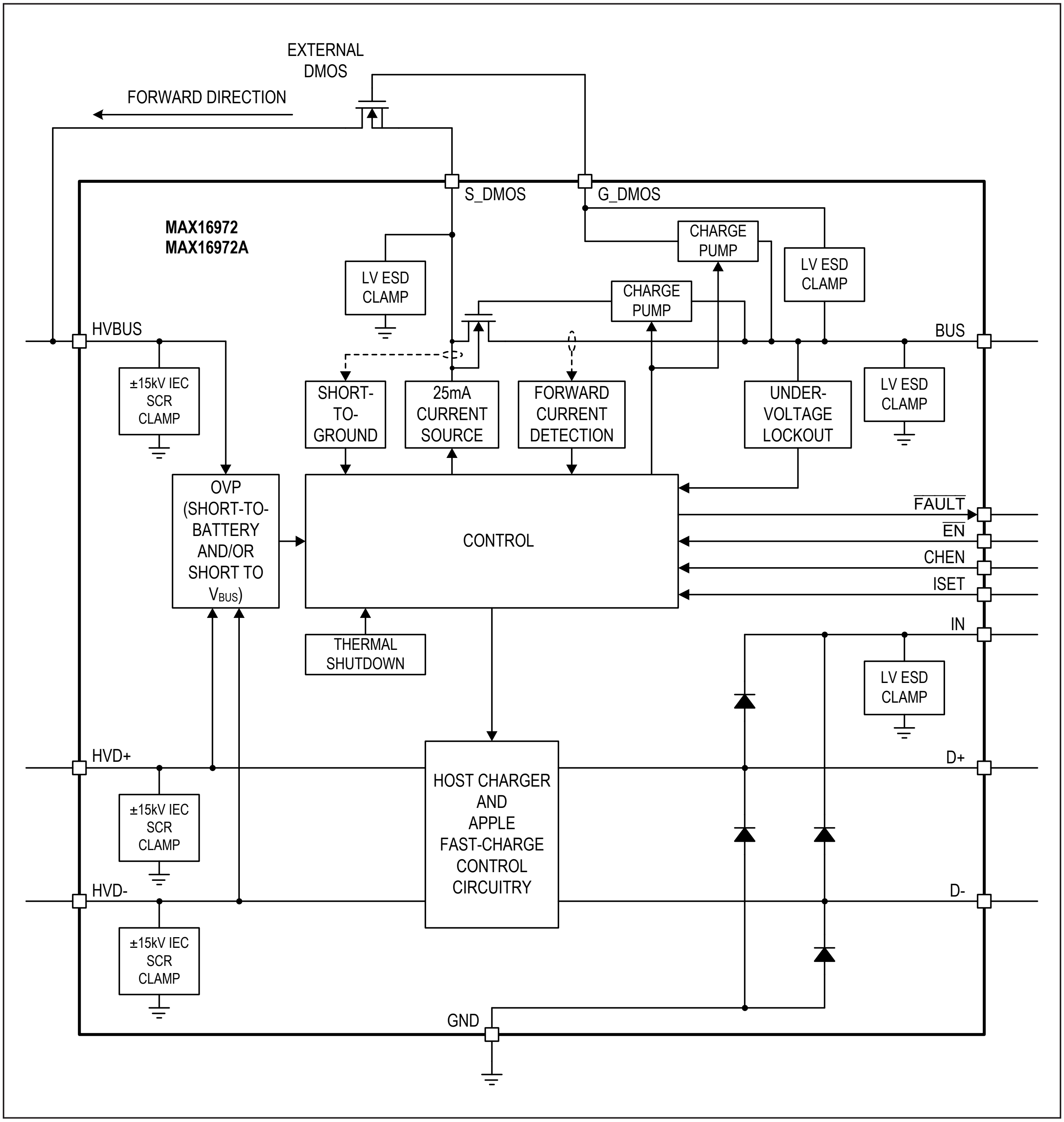
Benefits and Features

- 900MHz Bandwidth USB 2.0 Data Switches
- Industry-Leading $R_{DS(ON)}$ Minimizes Voltage Drop on Bus Line to Help Meet USB Voltage Specifications at Device Connector
  - Current-Limited 31mΩ (typ) BUS Switch with High-Capacitive Load Capability
- Robust Overvoltage and ESD Protection for Automotive Environment Saves on External Protection Components
  - Short-to-Battery and Short-to-GND Protection on Protected HVBUS Output
  - Short-to-Battery and Short-to-HVBUS Protection on Protected HVD+ and HVD- Outputs
  - Two 4.0Ω (typ) R_{ON} USB 2.0 Data Switches
  - Integrated Overcurrent and Short-Circuit Autoretry
  - High ESD Protection (HVD+, HVD-, HVBUS)
    - ±15kV Human Body Model
    - ±15kV IEC 61000-4-2 Air Gap
    - ±8kV IEC 61000-4-2 Contact
  - 20ms Fault-Blanking Timeout Period
- Automatic Transitioning of Charge Modes through Intelligent State Machine for Seamless Device Integration
  - Integrated Apple iPhone 1.0A Dedicated Charging Mode
  - Integrated Apple iPad 2.1A Dedicated Charging Mode
  - USB-IF BC1.2 Charging Downstream Port (CDP) and Dedicated Charging Port (DCP) Modes
  - Chinese Telecommunication Industry-Standard YD/T 1591-209
  - USB On-The-Go (OTG) Support
- AEC-Q100 Qualified

Typical Operating Circuit and Ordering Information appear at end of data sheet.

Simplified Block Diagram



Absolute Maximum Ratings

IN, BUS, ISET, S_DMOS to GND ....-0.3V to +6V
D+, D- to GND ....-0.3V to IN +0.3V
EN, $\overline{EN}$, $\overline{FAULT}$, CHEN to GND ....-0.3V to +6V
HVD+, HVD-, HVBUS to GND ....-0.3V to +18V
G_DMOS to GND...-0.3V to +16V
Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 9.5mW/°C above +70°C).....................761mW
TQFN (derate 25mW/°C above +70°C)....................2000mW

Operating Temperature Range......................... -40°C to +105°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering) (10s)...............................+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 QSOP

Package Code	E16+11C
Outline Number	21-0055
Land Pattern Number	90-0167
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	105°C/W
Junction to Case (θ_{JC})	37°C/W

16 TQFN

Package Code	T1644+4C
Outline Number	21-0139
Land Pattern Number	90-0070
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	40°C/W
Junction to Case (θ_{JC})	6°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{BUS} = 5.0V, V_{IN} = 3.3V, T_J = T_A = -40°C to +105°C, R_L = ∞, Typical values are at $V_{\overline{EN}}$ = 0V or V_{EN} = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
BUS Power-Supply Range	V_{BUS}		4.75		5.5	V
IN Power-Supply Range	V_{IN}		3		3.6	V
IN Overvoltage Lockout	V_{OVLO}	V_{IN} rising	3.8			V
BUS Input Current	I_{BUS}	Supply for internal blocks		572	1100	µA
		Shutdown, EN active-high versions, V_{IN} = 0V		2.5	5	
		Shutdown, $\overline{EN}$ active-low versions, V_{IN} = 0V		5	10	
IN Input Current	I_{IN}	V_{CHEN} = V_{IN} = 3.3V		3.3	10	µA
CHARGE PUMP						
Unloaded Output Voltage	V_{OCHP}	Referenced to V_{BUS}, internal discharge path 2MΩ to GND	8		10.5	V
Output Impedance	R_{OCHP}				50	kΩ
Output DC Current	I_{OCHP}	V_{G_DMOS} - V_{BUS} ≥ 7V	20			µA
D+/D- ANALOG USB SWITCHES						
Analog Signal Range		Guaranteed by R_{ON} measurement (Note 2)	0		3.6	V
Protection Trip Threshold	V_{OV_D}		3.7	3.85		V
Protection Response Time	t_{FP_D}	Delay to $V_{D\_}$ < 3V when $V_{HVD\_}$ = 3.3V to 4.3V step, R_L = 15kΩ on D_		6		µs
Overvoltage-Blanking Timeout Period	t_{B,OV_D}	From overvoltage condition to $\overline{FAULT}$ asserted		20		ms
On-Resistance	R_{ON}	V_{BUS} = 5V, I_L = 10mA, 0V ≤ $V_{D\_}$ ≤ 3.6V		4		Ω
On-Resistance Match Between Channels, Switch A	ΔR_{ON}	V_{BUS} = 5V, I_L = 10mA, $V_{D\_}$ = 1.5V, or 3.0V		0.03	0.2	Ω
On-Resistance Flatness, Switch A	$R_{FLAT(ON)}$	V_{BUS} = 5V, I_L = 10mA, $V_{D\_}$ = 0V or 0.4V		0.02		Ω
On-Resistance of HVD+/HVD- Short	R_{SHORT}	V_{DP} = 1V, I_{DM} = 500µA		90	180	Ω
HVD+/HVD- Off-Leakage Current	I_{D_OFF}	$V_{HVD\_}$ = 18V, $V_{D\_}$ = 0V, T_A = +25°C		60	120	µA
HVD+/HVD- On-Leakage Current	I_{D_ON}	$V_{D\_}$ = V_{IN} or 0V, device enabled, T_A = +25°C		7		µA
D+/D- Off-Leakage Current	I_{D_OFF}	$V_{HVD\_}$ = 18V, $V_{D\_}$ = 0V, T_A = +25°C		1		µA
On-Channel -3dB Bandwidth	BW	R_L = 50Ω, source impedance = 50Ω; see Figure 5 in the *Timing Diagrams/Test Circuits* section		900		MHz
Crosstalk	V_{CT}	R_L = 50Ω, f = 480MHz		-30		dB

Electrical Characteristics (continued)

(V_{BUS} = 5.0V, V_{IN} = 3.3V, T_J = T_A = -40°C to +105°C, R_L = ∞, Typical values are at $V_{\overline{EN}}$ = 0V or V_{EN} = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On-Capacitance	C_{ON}	f = 1MHz		10		pF
Rise-Time Propagation Delay	t_{PLH}	R_S = R_L = 50Ω		200		ps
Fall-Time Propagation Delay	t_{PHL}	R_S = R_L = 50Ω		200		ps
Output Skew Between Switches	$t_{SK(O)}$	Skew between D+ and D- switch, R_L = 50Ω		50		ps
Output Skew Same Switch	$t_{SK(P)}$	Skew between opposite transitions in same switch, R_L = 50Ω		50		ps
BUS POWER SWITCH						
V_{BUS} Toggle Time	t_{VBT}	Going into and out of DCP/Apple autodetection modes	0.5	1	2	s
HVBUS Protection Trip Threshold Absolute	$V_{OV\_BUS,ABS}$	HVBUS rising	5.6	5.8		V
HVBUS Protection Trip Threshold Relative	$V_{OV\_BUS,REL}$	HVBUS rising		V_{BUS} + 0.10V		V
Voltage Protection Response Time	t_{FP_BUS}	HVBUS rising		0.3		µs
Overvoltage-Fault Blanking Timeout Period	t_{BOV_BUS}	From overvoltage condition to $\overline{FAULT}$ asserted	10	20	35	ms
BUS Undervoltage Lockout	V_{UVLO}	V_{BUS} falling			4.2	V
BUS Undervoltage Protection	V_{UV_BUS}	V_{BUS} falling from 5V with slew rate of 0.5V/µs, switch turned off (with R_L = 50Ω on S_DMOS measured when S_DMOS goes low)	4.3	4.45	4.6	V
BUS Undervoltage-Protection Response Time	t_{F_BUS}	V_{BUS} falling from 5V with slew rate of 0.5V/µs, switch turned off (with R_L = 50Ω on S_DMOS measured when S_DMOS goes low)		1		µs
BUS Undervoltage-Protection Fault-Blanking Timeout Period	t_{B,UV_BUS}	From undervoltage condition to $\overline{FAULT}$ asserted		20		ms
On-Resistance	R_{ON}			31	50	mΩ
Forward Current Limit	I_{LIM}	R_{ISET} = 51.1kΩ, V_{BUS} - V_{S_DMOS} = 0.5V	0.6	0.67	0.82	A
		R_{ISET} = 26.7kΩ, V_{BUS} - V_{S_DMOS} = 0.5V	1.25	1.36	1.47	
		R_{ISET} = 15.4kΩ, V_{BUS} - V_{S_DMOS} = 0.5V	2.1	2.37	2.47	
		R_{ISET} = 10.0kΩ, V_{BUS} - V_{S_DMOS} = 0.5V (Note 3)	3.12	3.63	4.28	
Voltage at ISET	V_{ISET}		1.18	1.24	1.3	V
ISET Short-Detection Threshold	$I_{ISET,SC}$	Switch turned off when current at ISET exceeds value	180	300	480	µA

Electrical Characteristics (continued)

(V_{BUS} = 5.0V, V_{IN} = 3.3V, T_J = T_A = -40°C to +105°C, R_L = ∞, Typical values are at $V_{\overline{EN}}$ = 0V or V_{EN} = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Current-Limit Fault-Blanking Timeout Period	$t_{B,ILIM}$	From continuous current-limit condition to $\overline{FAULT}$ asserted		20		ms
HVBUS Turn-On Delay	t_{ON}	From 0 to 10% of V_{OUT}		0.6		ms
HVBUS Output Rise Time	t_{RISE}	From 10% to 90% of V_{OUT}		0.4		ms
HVBUS Turn-Off Delay	t_{OFF}	From 100% to 90% of V_{OUT}		1.3		ms
HVBUS Output Fall Time	t_{FALL}	From 90% to 10% of V_{OUT}		1.2		ms
HVBUS OUT Autoreset Current	I_{RETRY}	In latched-off state, V_{HVBUS} = 0V		25		mA
HVBUS OUT Autoreset Threshold	V_{RETRY}	In latched-off state, V_{HVBUS} rising		0.5		V
HVBUS OUT Autoreset Blanking Time	$t_{B,RETRY}$	In latched-off state, V_{HVBUS} > 0.5V		20		ms
Off-Leakage Current	I_{LKG_HVBUS}	V_{HVBUS} = 18V, V_{BUS} = 4.75V, T_A = +25°C		30	65	µA
S_DMOS Off-Leakage Current		V_{BUS} = 5.5V, VS_DMOS = 0V, TA = +25°C		1		µA
THERMAL PROTECTION						
Thermal Shutdown				160		°C
Thermal-Shutdown Hysteresis				20		°C
$\overline{FAULT}$ OUTPUT						
$\overline{FAULT}$ Output Low Voltage	V_{OL}	I_{SINK} = 500µA			0.1	V
$\overline{FAULT}$ Output High Leakage		T_A = +25°C		1		µA
EN/$\overline{EN}$, IN, CHEN INPUTS						
Input Logic-High	V_{IH}		1.6			V
Input Logic-Low	V_{IL}				0.5	V
Input Current EN, CHEN	I_{EN}, I_{CHEN}	V_{IN}, internal 2MΩ pulldown to GND		1.65		µA
Input Current EN	$I_{\overline{EN}}$	$\overline{EN}$, active-low versions, V_{IN} = 0V, internal 2MΩ pullup to BUS		-1.65		µA
USB HOST CHARGING SPEC, D+/D-/CHEN (CDP)						
HVDP and HVDM Pulldown Resistors	R_{HVD_DWN}			19		kΩ
Input Logic-High	V_{IH}		2			V
Input Logic-Low	V_{IL}				0.8	V
Data Sink Current	I_{DAT_SINK}	V_{DAT_SINK} = 0.25V to 0.4V; includes 19kΩ (typ) pulldown resistor	45		175	µA

Electrical Characteristics (continued)

(V_{BUS} = 5.0V, V_{IN} = 3.3V, T_J = T_A = -40°C to +105°C, R_L = ∞, Typical values are at $V_{\overline{EN}}$ = 0V or V_{EN} = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data-Detect Voltage High	V_{DAT_REFH}		0.4			V
Data-Detect Voltage Low	V_{DAT_REFL}				0.25	V
Data-Detect Voltage Hysteresis	V_{DAT_HYST}			60		mV
Data-Source Voltage	V_{DAT_SRC}	I_{LOAD} = 200µA	0.5		0.7	V
iPHONE/iPAD/DCM CHARGER DETECTION (DCP)						
HVD+/HVD- Short Pulldown	R_{PD}		300	500		kΩ
RP1/RP2 Ratio	RT_{RP}			1.5		Ω/Ω
RP1 || RP2 Resistance	R_{RP}		19.5	30	40.5	kΩ
RM1/RM2 Ratio	RT_{RM}			0.86		Ω/Ω
RM1 || RM2 Resistance	R_{RM}		15.1	23.2	31.3	kΩ
DM1 Comparator Threshold	V_{DM1F}	iPhone mode, DM falling	45	46	47	% (V_{BUS})
		iPad mode, DM falling	29	30	31	
DM2 Comparator Threshold	V_{DM2F}	DM falling	6	7	8	% (V_{BUS})
DP Comparator Threshold	V_{DM1F}	iPhone mode, DP rising	45	46	47	% (V_{BUS})
		iPad mode, DP rising	55.9	57.2	58.5	
DM1, DM2, and DP Comparator Hysteresis				1		%
ESD PROTECTION FOR ALL INPUTS AND OUTPUTS EXCEPT HVD+, HVD-, AND HVBUS						
ESD Protection Level	V_{ESD}	Human Body Model		±2		kV
ESD PROTECTION FOR HVD+, HVD-, HVBUS						
ESD Protection Level	V_{ESD}	ISO 10605 Air Gap (330pF, 2kΩ)		±25		kV
		ISO 10605 Contact (330pF, 2kΩ)		±8		
		IEC 61000-4-2 Air Gap (150pF, 330Ω)		±25		
		IEC 61000-4-2 Contact (150pF, 330Ω)		±8		
		IEC 61000-4-2 Air Gap (330pF, 330Ω)		±15		
		IEC 61000-4-2 Contact (330pF, 330Ω)		±8		

Note 1: Specifications with minimum and maximum limits are 100% production tested at T_A = +25°C and are guaranteed over the operating temperature range by design and characterization. Actual typical values may vary and are not guaranteed.
Note 2: Design guaranteed by ATE characterization. Limits are not production tested.
Note 3: Design guaranteed by bench characterization. Limits are not production tested.

Timing Diagrams/Test Circuits

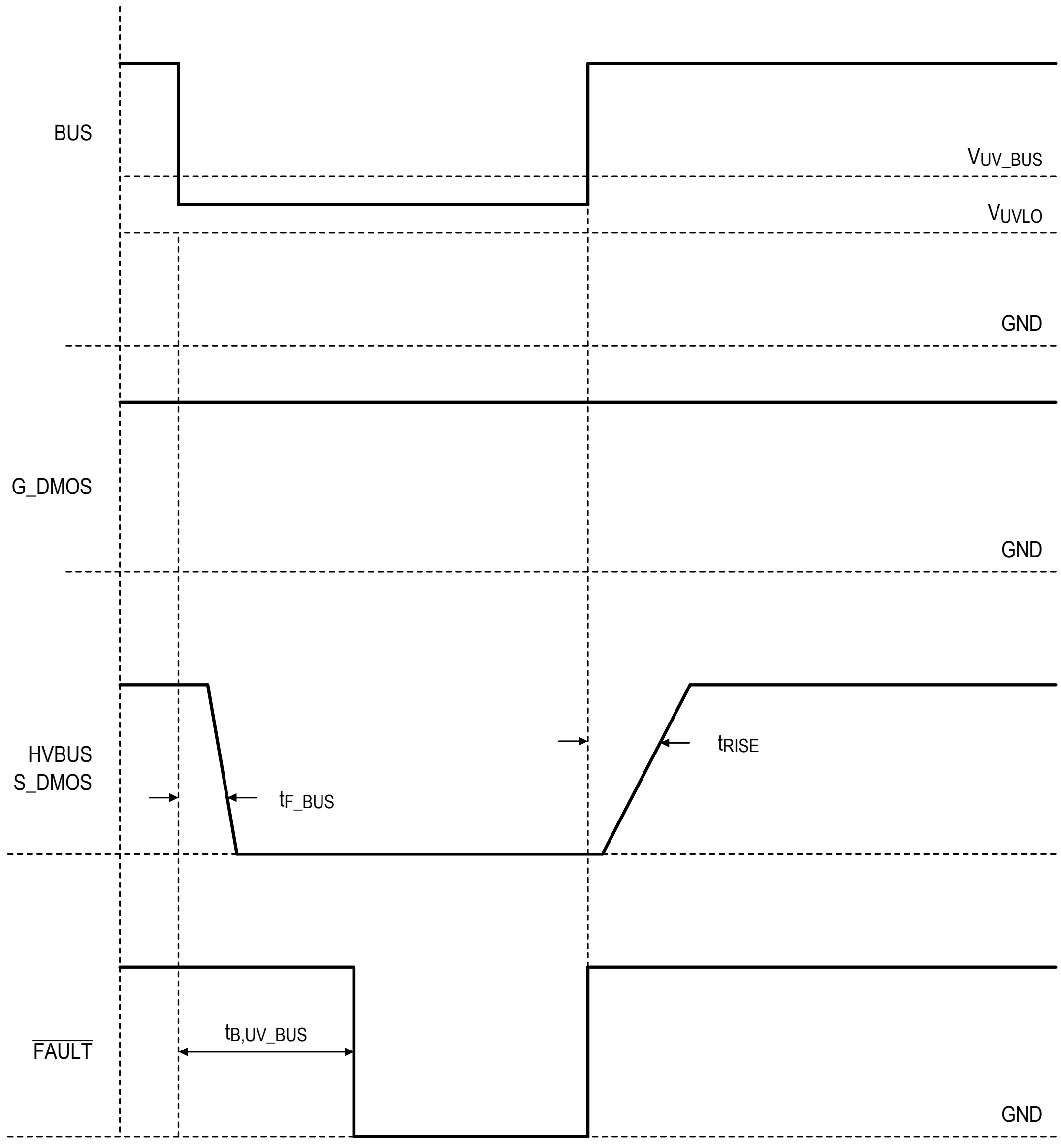


Figure 1. BUS Undervoltage Event

Timing Diagrams/Test Circuits (continued)

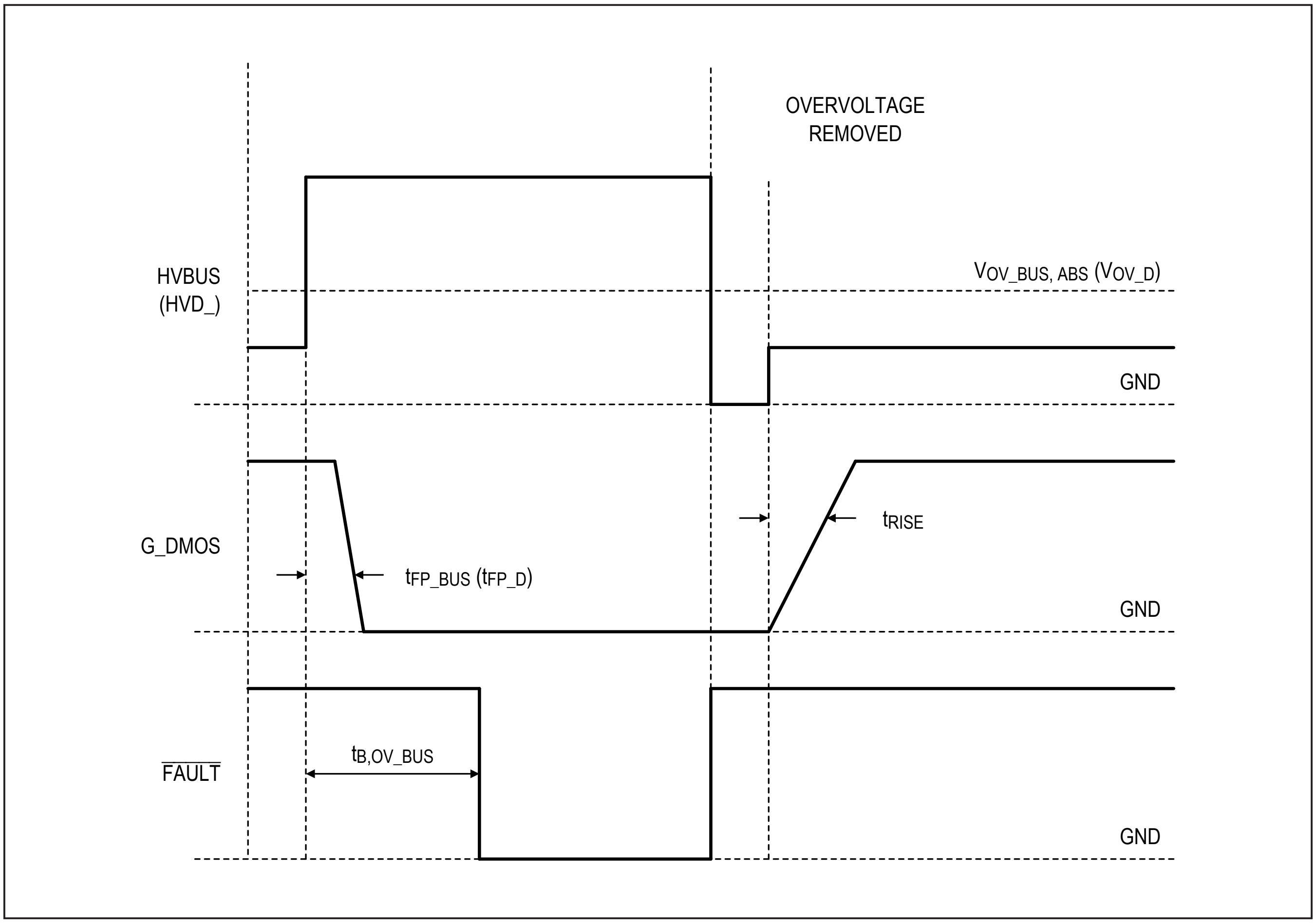


Figure 2. Overvoltage Protection Event

Timing Diagrams/Test Circuits (continued)

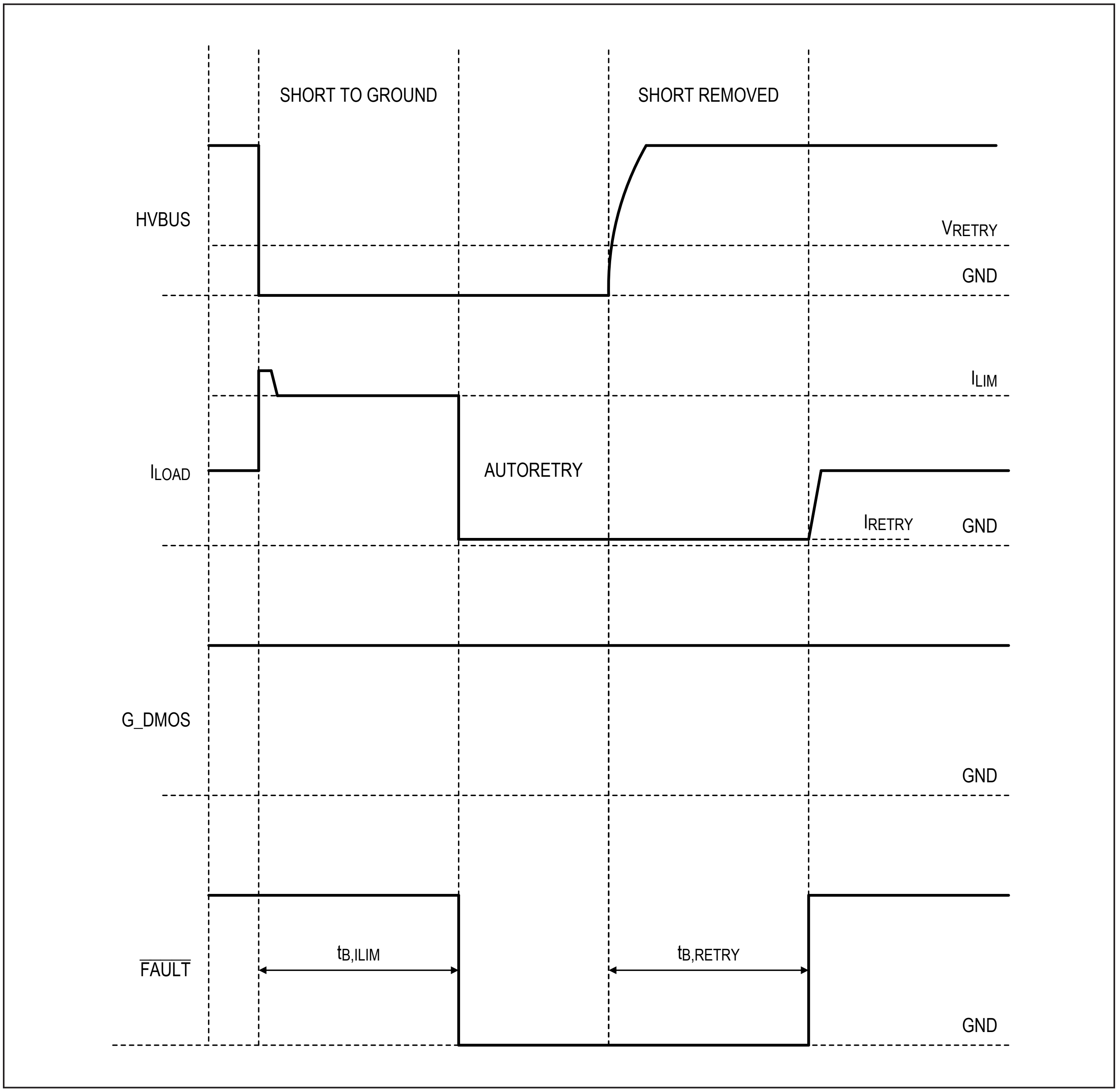


Figure 3. Short-to-Ground Protection Event

Timing Diagrams/Test Circuits (continued)

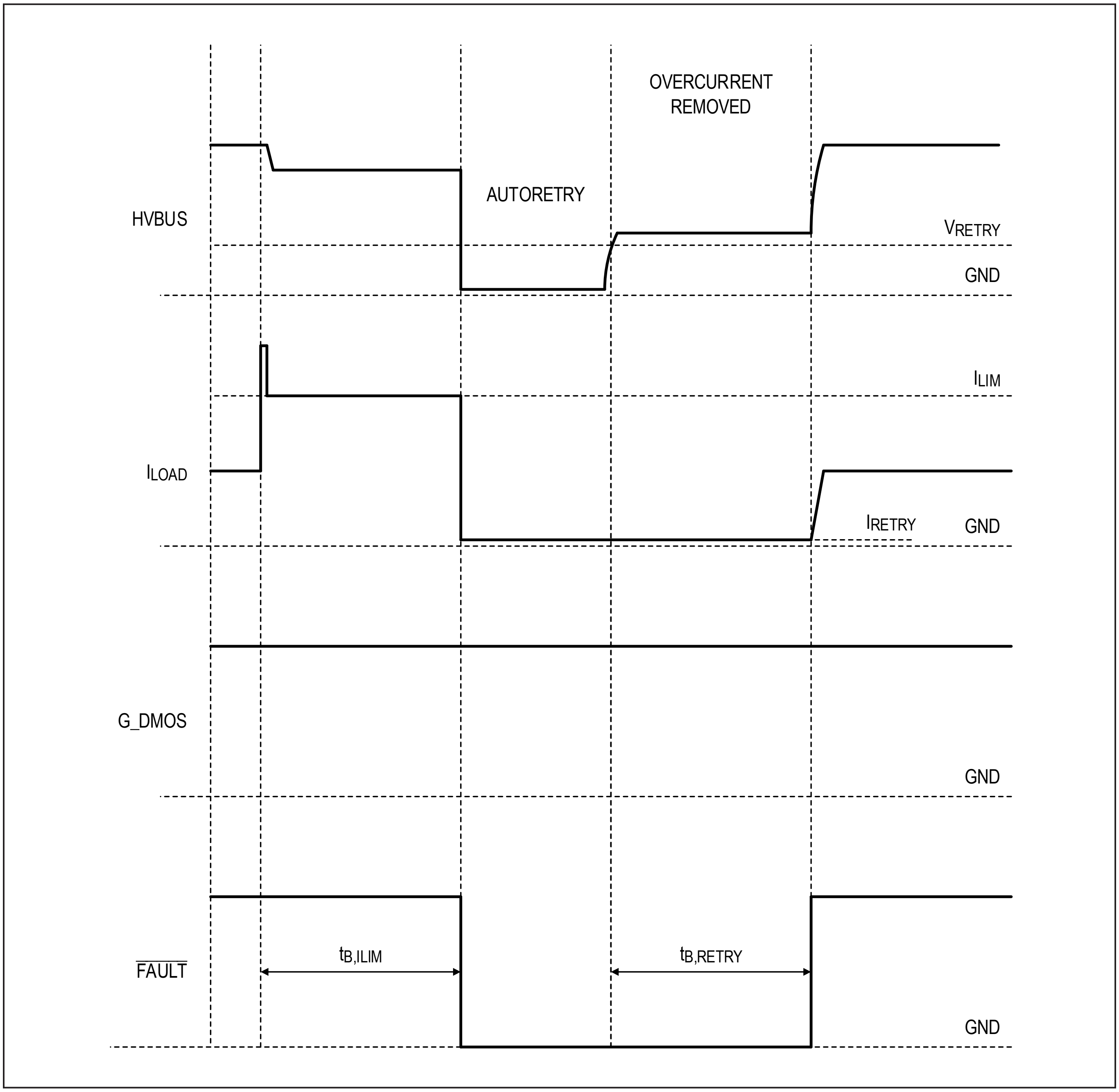


Figure 4. Overcurrent Protection Event

Timing Diagrams/Test Circuits (continued)

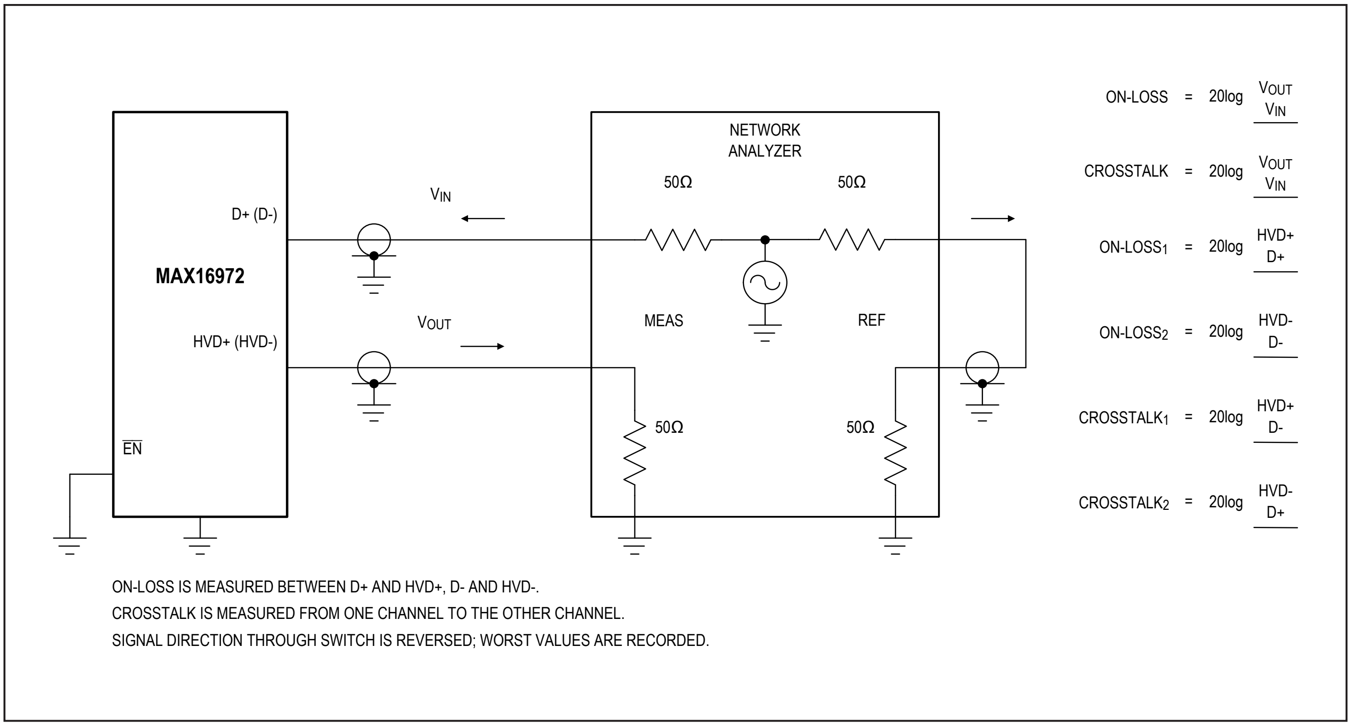


Figure 5. In-Channel -3dB Bandwidth and Crosstalk

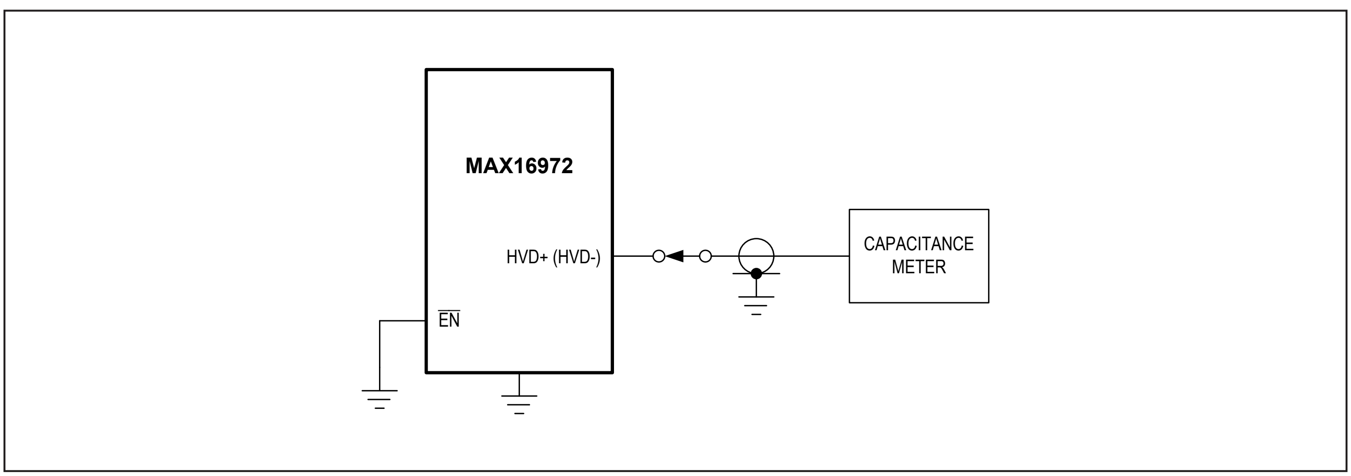


Figure 6. On-Capacitance

Timing Diagrams/Test Circuits (continued)

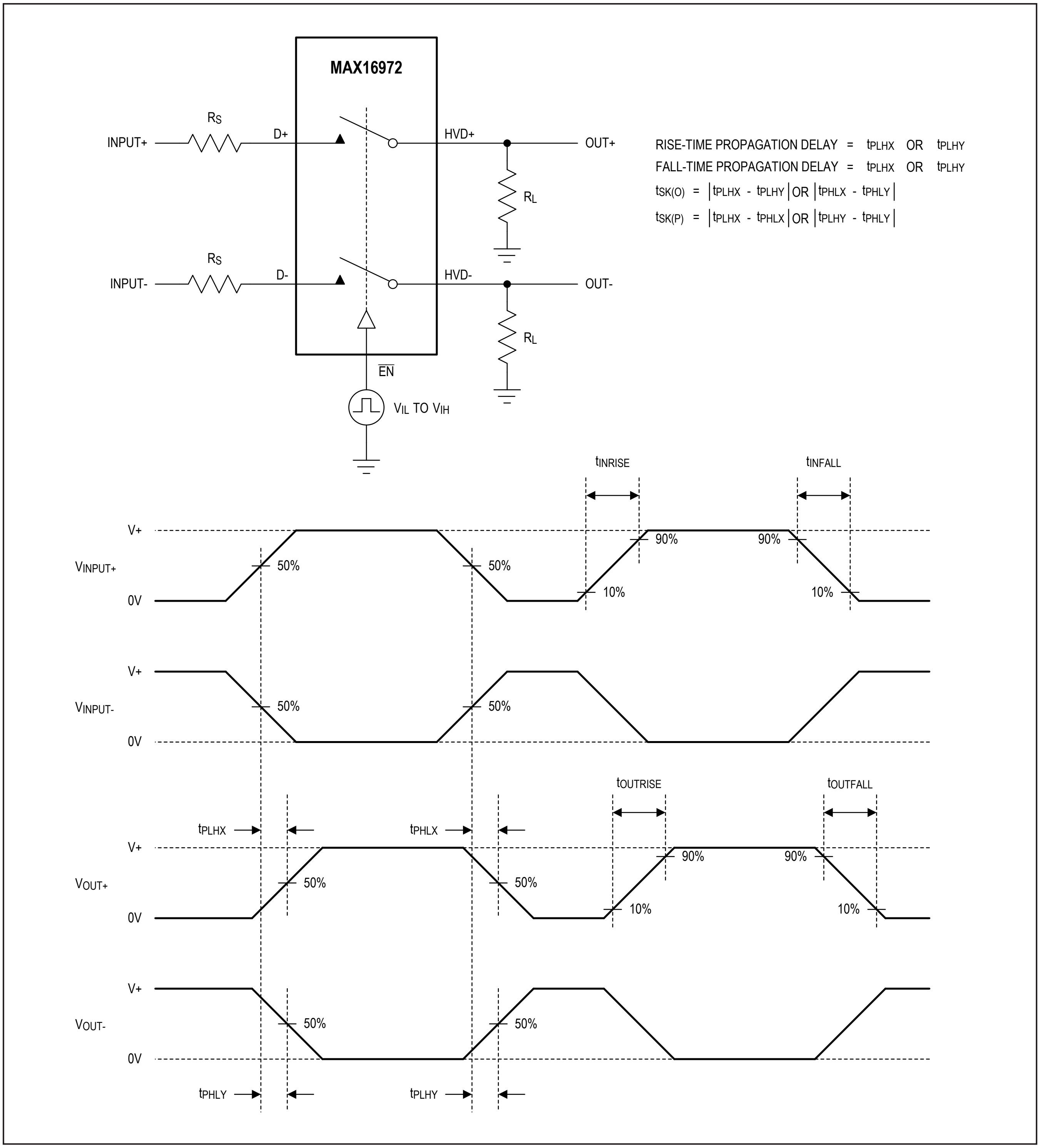
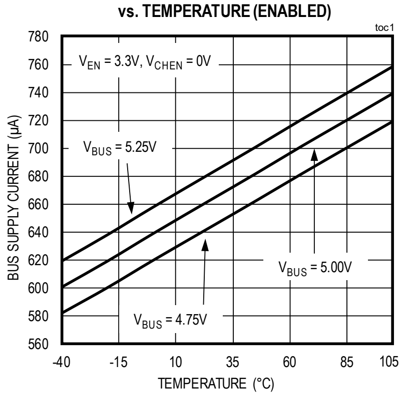


Figure 7. Propagation Delay and Output Skew

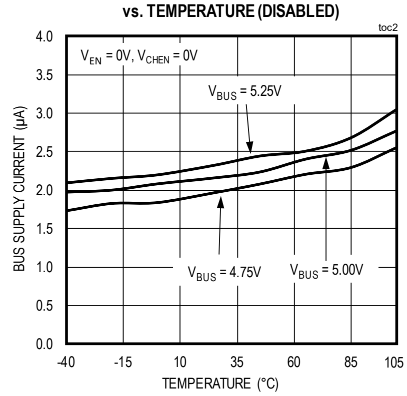
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

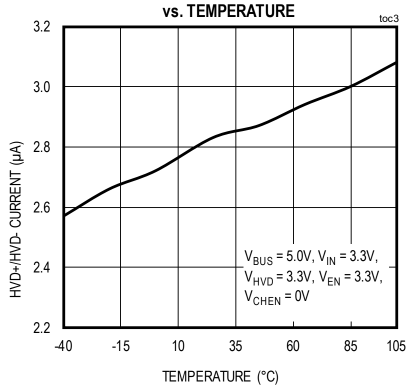
BUS SUPPLY CURRENT vs. TEMPERATURE (ENABLED)



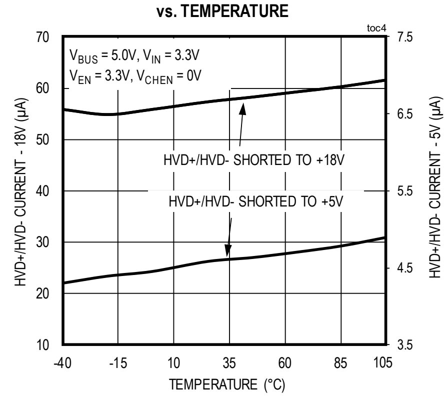
BUS SUPPLY CURRENT vs. TEMPERATURE (DISABLED)



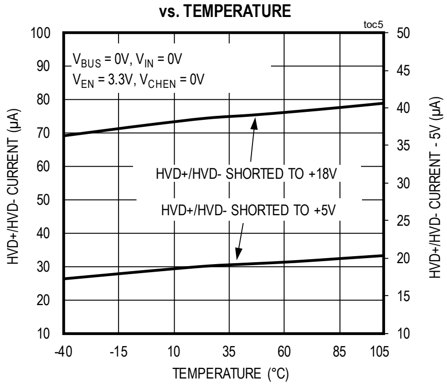
HVD+/HVD- LEAKAGE CURRENT vs. TEMPERATURE



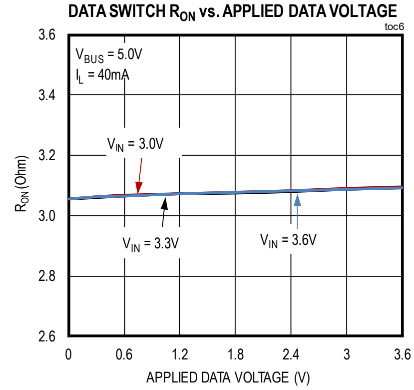
HVD+/HVD- LEAKAGE CURRENT vs. TEMPERATURE



HVD+/HVD- LEAKAGE CURRENT vs. TEMPERATURE



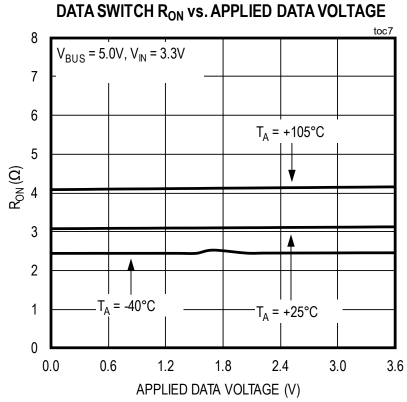
DATA SWITCH R_{ON} vs. APPLIED DATA VOLTAGE



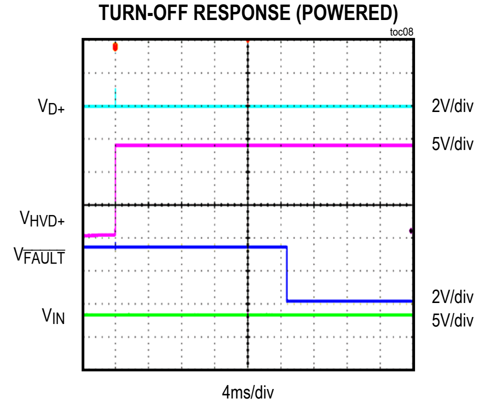
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

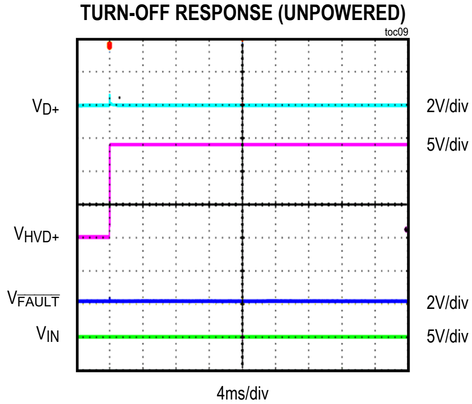
DATA SWITCH R_{ON} vs. APPLIED DATA VOLTAGE



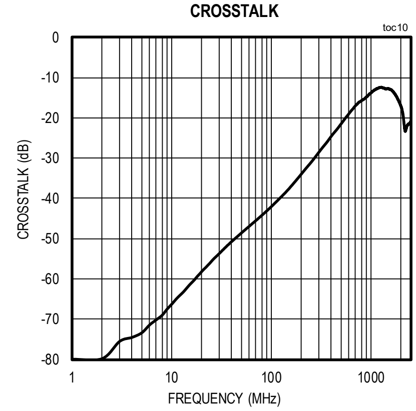
HVD± SHORT-TO-BATTERY TURN-OFF RESPONSE (POWERED)



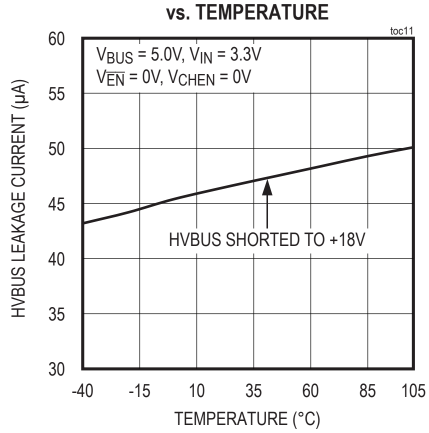
HVD± SHORT-TO-BATTERY TURN-OFF RESPONSE (UNPOWERED)



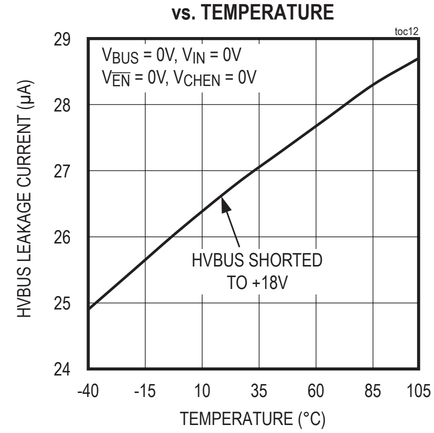
CROSSTALK



HVBUS LEAKAGE CURRENT vs. TEMPERATURE



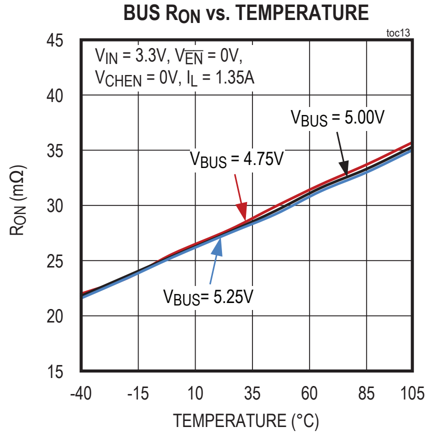
HVBUS LEAKAGE CURRENT vs. TEMPERATURE



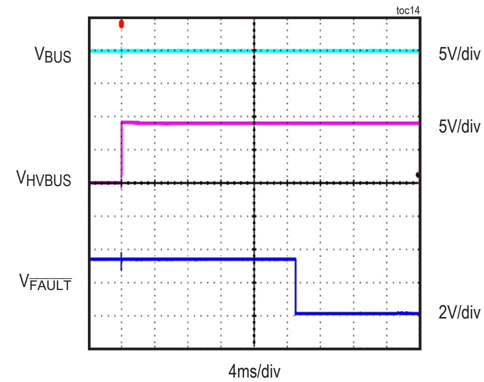
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

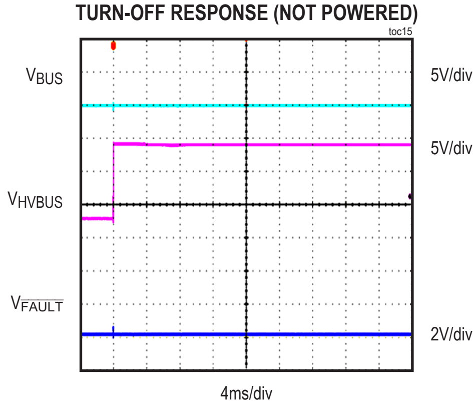
BUS R_{ON} vs. TEMPERATURE



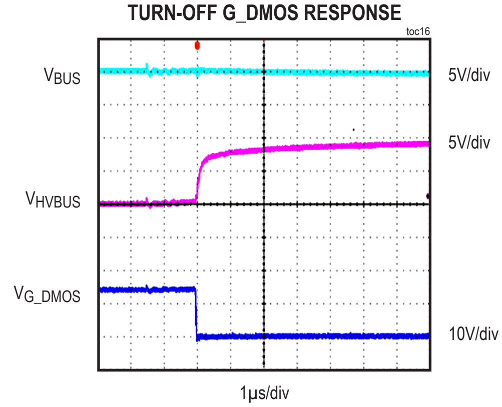
HVBUS SHORT-TO-BATTERY TURN-OFF RESPONSE



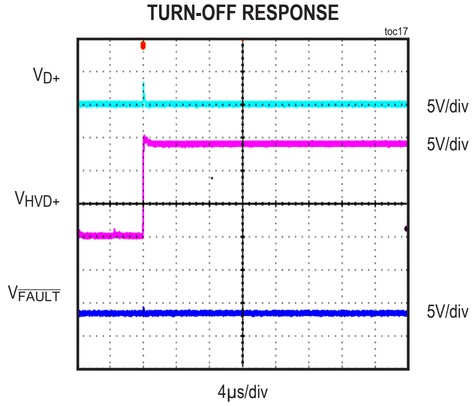
HVBUS SHORT-TO-BATTERY TURN-OFF RESPONSE (NOT POWERED)



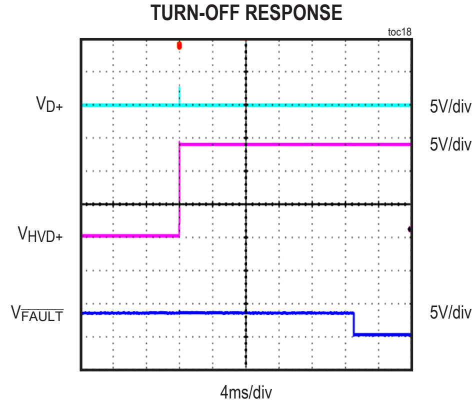
HVBUS SHORT-TO-BATTERY TURN-OFF G_DMOS RESPONSE



HVD± SHORT-TO-BATTERY TURN-OFF RESPONSE



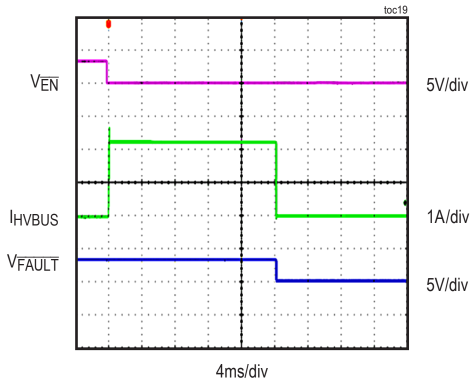
HVD± SHORT-TO-BATTERY TURN-OFF RESPONSE



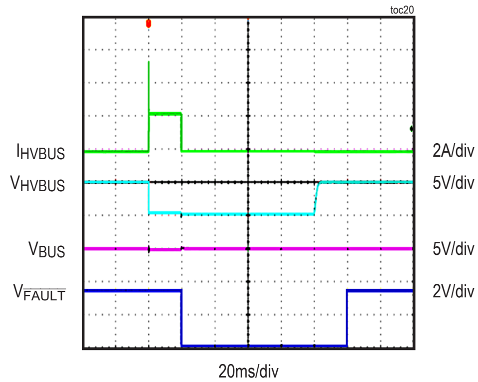
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

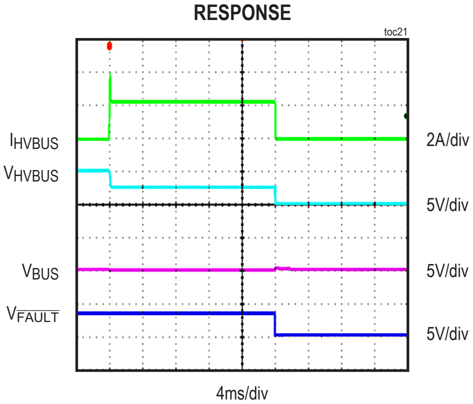
DEVICE ENABLED INTO SHORT-TO-GROUND



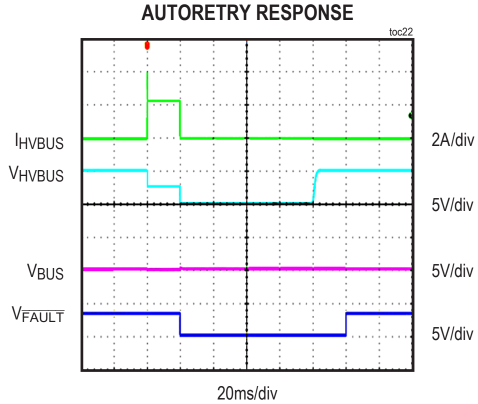
HVBUS SHORT-CIRCUIT AUTORETRY RESPONSE



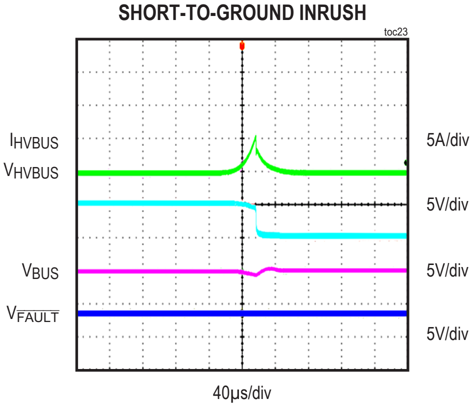
HVBUS OVERCURRENT RESPONSE



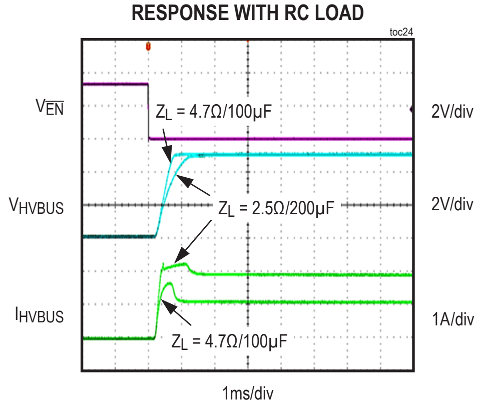
HVBUS OVERCURRENT AUTORETRY RESPONSE



SHORT-TO-GROUND INRUSH

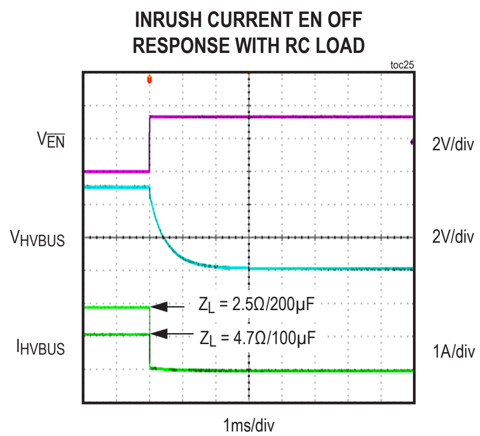


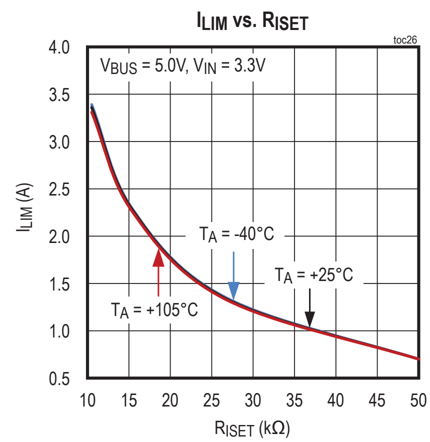
INRUSH CURRENT EN ON RESPONSE WITH RC LOAD

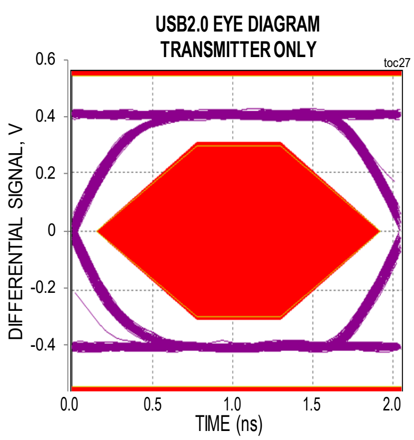


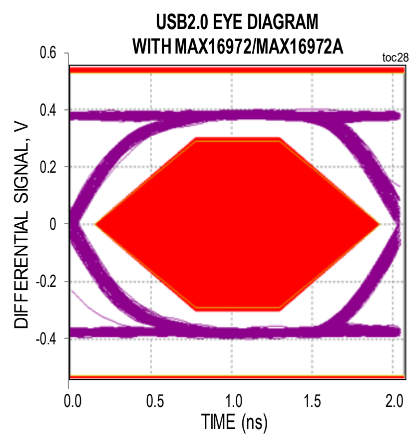
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

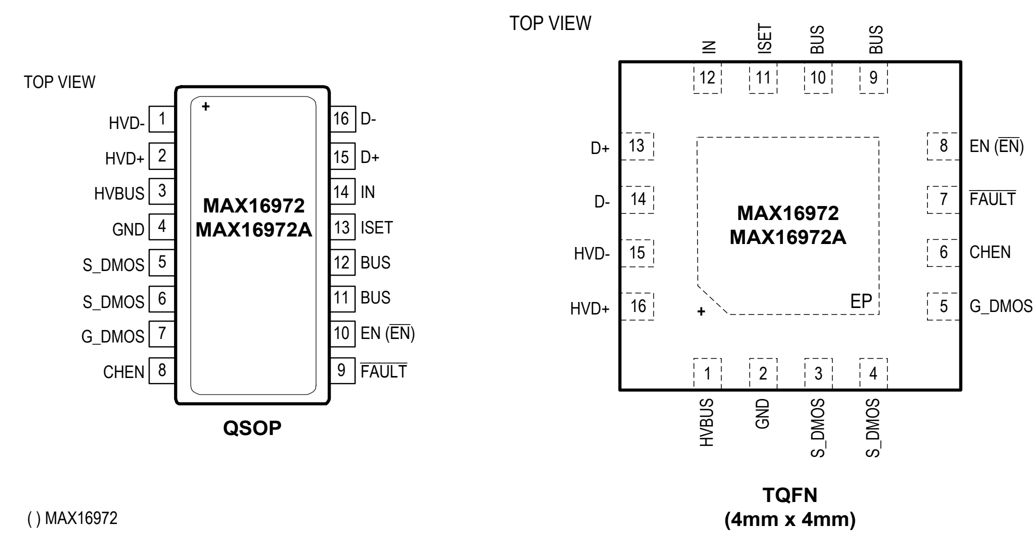








Pin Configurations



Pin Description

PIN	NAME	FUNCTION
1	HVD-	High-Voltage-Protected USB Differential Data D- Output. Connect HVD- directly to USB connector D-.
2	HVD+	High-Voltage-Protected USB Differential Data D+ Output. Connect HVD+ directly to USB connector D+.
3	HVBUS	High-Voltage Bus and DMOS Drain Connect. Connect to the drain of an external n-channel DMOS and to the USB connector BUS.
4	GND	Ground
5, 6	S_DMOS	DMOS Source Input. Connect to the source of an external n-channel DMOS. Connect both S_DMOS pins together and bypass S_DMOS to GND with a 100nF ceramic capacitor placed close to the S_DMOS pin.
7	G_DMOS	DMOS Gate-Drive Output. Connect to the gate of an external n-channel DMOS.
8	CHEN	Charger-Detect Configuration Bit 1. Connect CHEN to a microprocessor I/O (see Table 2 and Table 3).
9	$\overline{\text{FAULT}}$	Active-Low Open-Drain Fault Indicator Output
10	EN	MAX16972A - Active-High Charge-Detect Configuration Bit 0. Connect EN to a microprocessor I/O. Drive EN high to enable the device (see Table 2 and Table 3).
10	$\overline{\text{EN}}$	MAX16972 - Active-Low Charge-Detect Configuration Bit 0. Connect EN to a microprocessor I/O. Drive EN low to enable the device (see Table 2 and Table 3).
11, 12	BUS	USB Power Supply. Connect BUS to +5V USB supply. Connect both BUS inputs together for proper operation. Bypass BUS to GND with a 100µF ceramic capacitor.
13	ISET	Forward-Current Limit Set. Set the forward-current limit of the power switch using a resistor to GND (see the *Forward-Current Limit* section).
14	IN	Logic Power-Supply Input. The supply voltage range is from +3.0V to +3.6V. Bypass IN to GND with a 1µF ceramic capacitor.
15	D+	USB Differential Data D+ Input. Connect D+ to low voltage USB transceiver D+.
16	D-	USB Differential Data D- Input. Connect D- to low voltage USB transceiver D-.

Detailed Description

The MAX16972/MAX16972A provide high-ESD and short-circuit protection for the low-voltage internal USB data and USB power line in automotive radio, navigation, connectivity, and USB hub applications. Each device supports both Hi-Speed USB (480Mbps) and full-speed USB (12Mbps) operation. In addition, they also include integrated circuitry to enable fast-charging for consumer devices adhering to either the Apple method or the Hi-Speed USB host-charger port-detection protocol.

The short-circuit protection features include short-to-battery on the protected HVBUS, HVD+, and HVD- outputs, as well as short-to-HVBUS on the protected HVD+ and HVD- outputs. Each device is capable of a short-to-battery condition of up to +18V. Short-to-GND and overcurrent protection are also provided on the HVBUS output to protect the internal BUS power rail from overcurrent faults.

Each device features high-ESD protection to ±15kV Air-Gap method and ±8kV Contact method on all protected HVBUS, HVD+, and HVD- outputs.

Each device features two low 4.0Ω on-resistance Hi-Speed USB switches, a current-limited low-voltage 31mΩ BUS switch, and provides an integrated high-voltage external power-switch controller. The devices also feature an enable input, a fault output, integrated Apple iPhone/iPad fast-charging termination resistors, and an integrated host-charger port-detection circuit adhering to the USB 2.0 battery-charging specification.

BUS Protection

Power to the USB connector is provided through an externally controlled high-voltage FET and an internal, current-limited protected FET. The design can withstand short-to-battery conditions of up to 18V, short-to-ground, and can withstand the ±15kV (Air-Gap method)/±8kV (Contact method) ESD requirement. The internal FET has an adjustable current limit from 500mA up to 3A.

The HVBUS short-to-battery protection is done with an external power FET. The gate of this FET is driven by an internal charge pump which generates a minimum 7V gate-source voltage.

All overvoltage protection switches are guaranteed to be off when power is not applied to the device.

Fault Conditions

Table 1 summarizes the conditions that generate a fault and subsequent actions taken by the device.

Fault Output ($\overline{FAULT}$)

Each device features an active-low, open-drain fault output. $\overline{FAULT}$ goes low when there is a fault condition. Fault detection includes short-to-battery, short-to-GND, or overcurrent on HVBUS, overvoltage on HVD+ or HVD-, overheating in the device, and a low R_{ISET} value. Connect a 100kΩ pullup resistor from $\overline{FAULT}$ to IN.

Enable Input (EN/$\overline{EN}$)

Each device features either active-high or active-low enable logic (see the *Ordering Information* table). While V_{CHEN} = 0V, drive EN/($\overline{EN}$) high/(low) for normal operation and to enable the protection switches. This allows BUS power, D+, and D- USB signals to pass through the device. Drive EN/($\overline{EN}$) low/(high) to disable the device and to turn off the power and USB data switches (see Table 2 and Table 3).

Table 1. Fault Conditions

EVENT	CONDITION	ACTION TAKEN
Overvoltage on the High-Voltage Pins	V_{HVBUS} > (V_{BUS} + 0.1V) or 5.5V, V_{HVD+} or V_{HVD-} > 3.85V	• An overvoltage at one of the HVD pins immediately switches off all power and data switches. The blanking timer turns on and FAULT remains high. • If overvoltage persists for 20ms, FAULT goes low. • When the overvoltage is removed, the fault is cleared immediately, and FAULT goes high. • After the fault, the soft-start begins.
Overvoltage on IN	$V_{IN} > V_{OVLO}$	• The device immediately shuts off the external power switch and the USB data switches. The fault indicator asserts when the overvoltage condition persists for more than 20ms.
Overcurrent or Short-to-Ground on the High-Voltage Bus	$I_{LOAD} > I_{LIM}$	• If an overload occurs, output current regulates at ILIM and the blanking timer turns on. FAULT remains high during the blanking timeout period. • Continuous current at ILIM persists until either the 20ms blanking period expires, or a thermal fault occurs. • If overcurrent persists after 20ms, FAULT goes low, autoreset mode is enabled, and the output sources 25mA. • If the output voltage rises above 0.5V for 20ms, the channel resets, the output turns on, and FAULT goes high.
Undervoltage on BUS	$V_{UVLO} < V_{BUS} < V_{UV\_BUS}$	• A fast V_{BUS} UV immediately switches off the internal power switch. The blanking timer turns on and FAULT remains high. • If fast V_{BUS} UV persists for 20ms, FAULT goes low. • When the fast V_{BUS} UV is removed, the fault is cleared immediately and FAULT goes high. • After the fault, the soft-start begins.
	$V_{BUS} < V_{UVLO}$	• A V_{BUS} UVLO immediately switches off all power and data switches and resets the digital logic.
Overheating	T_J > +160°C	• The device immediately shuts off the external power switch, internal current-limited switch, and USB data switches. The fault indicator asserts immediately when the junction temperature exceeds +160°C. The device has a thermal hysteresis of 15°C. The fault indicator deasserts when the junction temperature falls below +145°C.
R_{ISET} Value Too Low	I_{ISET} > 300µA	• An ISET error immediately switches off all power and data switches. FAULT is asserted immediately. • When the ISET error is removed, the fault is cleared immediately and FAULT goes high.

CHEN Input

Use CHEN (along with EN/($\overline{EN}$); see Table 2 and Table 3) to enable the device's internal Apple iPhone/iPad fast-charge circuitry or the device's internal USB host-charger port-detection circuitry (Figure 8). The device's internal charge-detect circuitry allows any attached peripheral device to determine whether it is connected to a USB port capable of supplying greater than 500mA (typ). If detected, the peripheral device enables its internal battery charger to enter fast-charge mode, and begins charging above 500mA at its maximum capable current.

Connect CHEN to an I/O port on the host system microprocessor that has access to the USB transceiver. This is needed to place the device into one of its four operating modes: disabled, USB Hi-Speed (HS) mode, USB low-speed (LS)/full-speed (FS) mode with automatic host-charger port detection, and Apple iPhone/iPad fast-charging mode (Table 2 and Table 3).

For proper operation, the module system software must determine in which mode to place the device. When the consumer USB access port is idle (i.e., user selects playing FM, AM, or CD), the USB port could be placed in Apple iPhone fast-charging mode to rapid charge an Apple-compliant device. When the consumer USB port is active (i.e., user selects the USB port), the USB port must be placed in USB LS/FS mode with automatic host-charger port detection to begin normal operation.

Disable Mode

This is the lowest power mode for the device. In this mode, both the USB BUS power, HVD+ to D+ and HVD- to D-, data paths are disabled. The system software must select the disabled mode for a minimum of 100ms before entering or exiting the Apple iPhone/iPad fast-charging mode. This ensures a true hardware and software reset for the attached peripheral so that it can properly detect either normal operation or fast-charge mode upon power-up.

Modes of Operation

USB-IF Dedicated Charging Port (DCP) and Apple 2.1A with Autodetection

The devices feature an iPad/DCP autodetection mode for emulating dedicated iPad 2.1A charging and USB-IF dedicated charging ports (DCPs). See Table 2 and Table 3 for correct values of EN ($\overline{EN}$) and CHEN to activate the iPad/DCP autodetection mode. In this mode, the high-voltage-protected HVD+ and HVD- pins are disconnected from the low-voltage D+ and D- pins and are initially connected to internal resistor-dividers to provide the proper Apple-compliant iPad bias voltage. Data switches SA are opened and switches SB are closed (Figure 8). Initially, the iPad termination resistors are presented on the HVD± pins; the devices then monitor the voltages at HVD+ and HVD- to determine the type of device attached.

If the voltage at HVD- is +1.5V (typ) (V_{BUS} x 0.3) or higher and the voltage at HVD+ is +2.86V (typ) (V_{BUS} x 0.572) or lower, the state remains unchanged and the iPad termination resistors remain present.

If the voltage at HVD- is forced below the +1.5V (typ) (V_{BUS} x 0.3) threshold or if the voltage at HVD+ is forced higher than the +2.86V (typ) (V_{BUS} x 0.572) threshold, the internal switch disconnects HVD- and HVD+ from the resistor-divider (iPad switch open) and HVD+ and HVD- are shorted together for dedicated charging mode (S2 closed).

Once the charging voltage is removed, the short between HVD+ and HVD- is disconnected and the operation is restarted with the internal resistor-divider bias voltages appearing on HVD+ and HVD-.

USB-IF Dedicated Charging Port (DCP) and Apple 1A with Autodetection

Each device features an iPhone/DCP autodetection mode for emulating dedicated iPhone 1.0A charging and USB- IF dedicated charging ports (DCPs). See Table 2 and Table 3 for correct values of EN ($\overline{EN}$) and CHEN to activate iPhone/DCP autodetection mode. In this mode, the high-voltage-protected HVD+ and HVD- pins are disconnected from the low-voltage D+ and D- pins and are initially connected to internal resistor-dividers to provide the proper Apple-compliant iPhone bias voltage. Data switches SA are opened and switches SB are closed (Figure 8).

Initially, the iPhone termination resistors are presented on the HVD± pins. The devices then monitor the voltages at HVD+ and HVD- to determine the type of peripheral device attached.

If the voltage at HVD- is +2.3V (typ) (V_{BUS} x 0.46) or higher and the voltage at HVD+ is +2.3V (typ) (V_{BUS} x 0.46) or lower, the state remains unchanged and the iPhone termination resistors remain present.

If the voltage at HVD- is forced below the +2.3V (typ) threshold or if the voltage at HVD+ is forced higher than the +2.3V threshold, the internal switch disconnects HVD- and HVD+ from the resistor-divider (iPhone switch open) and HVD+ and HVD- are shorted together for dedicated charging mode (S2 closed).

Once the charging voltage is removed, the short between HVD+ and HVD- is disconnected and the operation is restarted with the internal resistor-divider bias voltages appearing on HVD+ and HVD-.

USB Low-Speed/Full-Speed (LS/FS) Mode with Automatic Host-Charger Port Protection

After a USB-compliant portable device detects V_{BUS}, it is allowed to check if the host device is a host charger by applying a voltage to HVD+ and checking the voltage on HVD-. At this time, it is assumed that HVD+ and HVD- are logic-low, which means that the voltage is less than 0.8V and CHEN is logic-high. The host charger port-detection circuit is then enabled (Figure 8).

When the portable device has connected in low-speed or full-speed mode, either D+ or D- is logic-high upon enumeration, which disables the automatic charger-detection circuit. The charger-detection circuitry is not enabled again until a USB disconnect is detected which ensures that USB communication is not interrupted by charger-detection circuitry.

USB Hi-Speed (HS) Mode

USB Hi-Speed (HS) mode provides true pass-through operation for USB Hi-Speed (480Mbps) data signals and disables the USB host-charger port-detection circuitry. See Table 2 and Table 3 for correct values of EN ($\overline{EN}$) and CHEN.

Table 2. MAX16972GEEA/V+, MAX16972GTEA/V+, MAX16972AGEEA/V+, MAX16972AGTEA/V+ Operation

CHEN	EN ($\overline{EN}$)	IN	SA	SB	MODE	USB +5V	DATA/CHARGE
0	1 (0)	3.3V	1	0	HS Mode	On	Data Only
0	0 (1)	3.3V	0	0	Disabled	Off	Off
1	1 (0)	3.3V	On if CDP = 0	On if CDP = 1	LS FS Mode with CDP Auto to HS Mode	On	Data + Auto Host Charging
1	0 (1)	3.3V	0	1	DCP/Apple 1A Autodetection	On	Data Off/Auto USB Host Charging and Apple 1A/ DCP Mode On
X	X	0V	0	0	Disabled	Off	Off

( ) For MAX16972; X = Don't care.

Note: *Operation described in this table is similar to MAX16969 to enable drop-in compatibility.*

Table 3. MAX16972GEEB/V+, MAX16972AGEEB/V+, MAX16972AGTEB/V+ Operation

CHEN	EN ($\overline{EN}$)	IN	SA	SB	MODE	USB +5V	DATA/CHARGE
0	1 (0)	3.3V	On if CDP = 0	On if CDP = 1	LS FS Mode with CDP Auto to HS Mode	On	Data + Auto Host Charging
0	0 (1)	3.3V	1	0	OTG Mode	Off	Data Only
1	1 (0)	3.3V	0	1	DCP/Apple 2.1A Autodetection	On	Data Off/Auto USB Host Charging and Apple 2.1A/DCP Mode On
1	0 (1)	3.3V	0	1	DCP/Apple 1A Autodetection	On	Data Off/Auto USB Host Charging and Apple 1A/ DCP Mode On
X	X	0V	0	0	Disabled	Off	Off

( ) For MAX16972; X = Don't care.

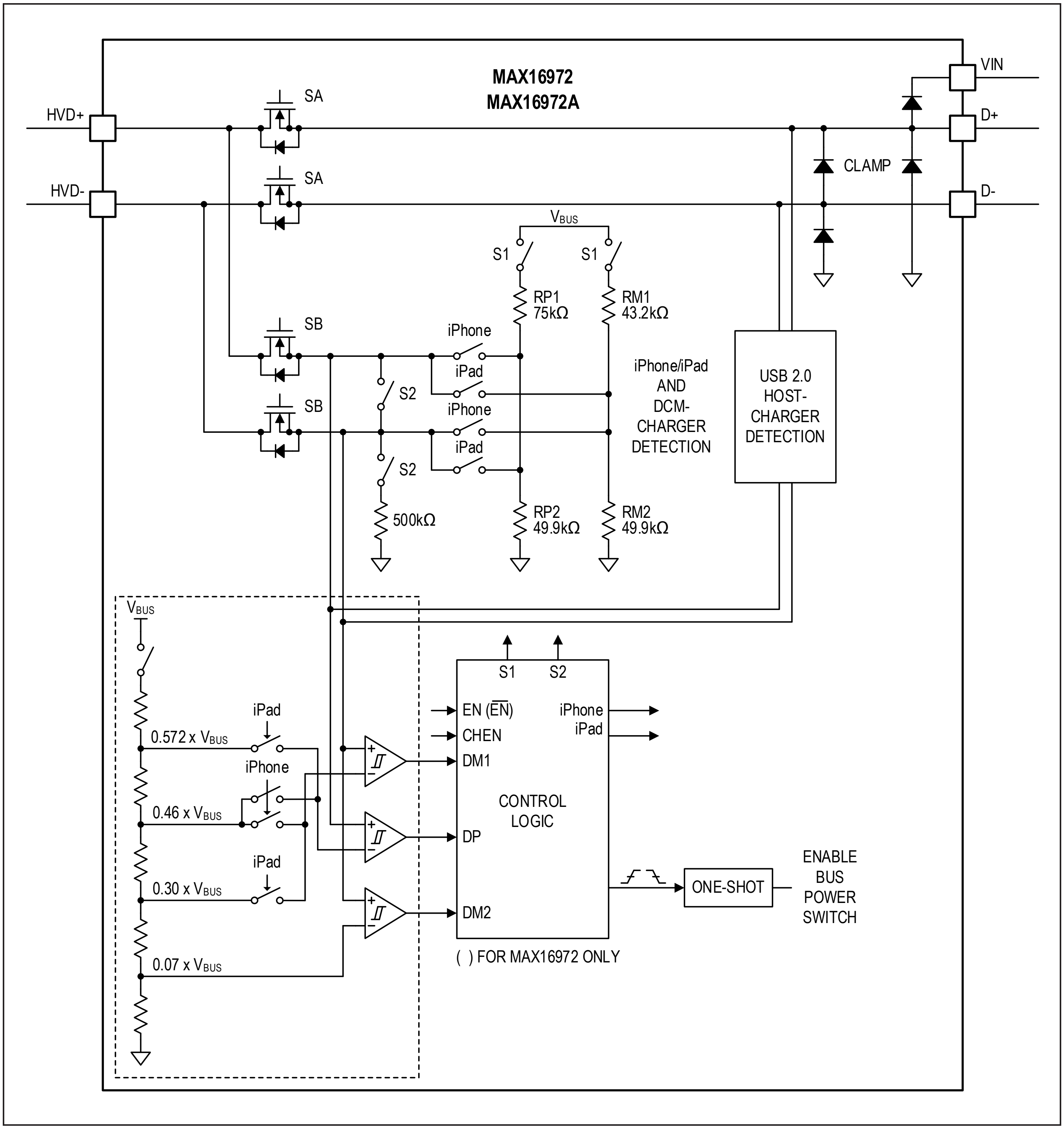


Figure 8. Host-Charger Port-Detection Circuit

Applications Information

Forward-Current Limit

Each device allows the current limit of the power switch to be set by a resistor. As shown in the forward-current limit specification of the *Electrical Characteristics* table, the typical current limit can vary by ±20% to ±25%. Assume variation of ±25% for forward-current limit between 500mA and 1A. For current limit above 1A, assume ±20% variation. The maximum expected current in the application determines the worst-case minimum current limit value to be set. It is recommended to have an additional 5% mar- gin to prevent triggering the current limit at the maximum expected current limit in the application. To find the correct value for R_{ISET}, modify the desired current limit value for the application ($I_{LIM,\ MIN}$) with a factor 1.33 (>1A) to 1.43 (<1A), which corresponds to the previously mentioned variations including the 5% margin.

Equation 1:

$$I_{LIM,\ TYP} = \text{factor} \times I_{LIM,\ MIN}$$

The resistor value is then calculated as: follows:

Equation 2:

$$R_{ISET} = 35{,}650/I_{LIM,\ TYP}$$

Examples for R_{ISET} are given in the *Electrical Characteristics* table and correspond to 0.5A, 1.2A, 2.1A, and 3.1A maximum current in the application.

The devices accommodate a forward current-limit range of 500mA to 3A. The short-circuit peak current limit is set 20% higher than the forward-current limit.

Selecting the External n-Channel DMOS Device

The external power DMOS device must be a 20V V_{GS} type. The charge pump generates approximately 7V V_{GS}, which guarantees low R_{ON} for nonlogic-level devices.

Power-Supply Bypass Capacitor

Bypass HVBUS to GND with a 0.1μF ceramic capacitor as close as possible to the USB connector to provide ±15kV (HBM) ESD protection. Parasitic inductance and capacitance due to long wire lengths between the load and HVBUS form an LC tank circuit, which can cause overshoots that violate absolute maximum ratings.

Ferrite beads to reduce EMI should be placed between the 0.1μF ceramic connector capacitor and the HVBUS node.

Connect a 1Ω resistor in series with a 10μF capacitor on the HVBUS node to GND to avoid overshoots on HVBUS. Bypass BUS to GND with a minimum 100μF, low-ESR ceramic capacitor to avoid large droops on BUS when hot plugging discharged capacitors on HVBUS. A capacitance of 100μF or more can already be present on the BUS net (i.e., from an upstream converter output). If this is the case, the MAX16972/MAX16972A do not require this 100μF bypass capacitor as long as the impedance between the existing capacitance and the BUS input pins is low enough to avoid a droop of 330mV at the USB receptacle during output current surges. For a HUB application, there is a minimum of 120μF per port in order to meet the USB specification.

Bypass IN to GND with 1μF ceramic capacitor. Place a 1kΩ resistor between the logic supply and IN node to ensure optimal ESD performance.

Wire Length

The wire length between USB peripheral and HVBUS, HVD+, and HVD- should each be in the range of 0.5m to 5m for proper operation. This length range corresponds to approximately 650nH to 6.5mH inductance. A minimum wire length is required for limiting the current slew rate for the short-to-battery and short-to-ground events.

Layout of USB Data Line Traces

USB Hi-Speed mode requires careful PCB layout with 90Ω controlled differential impedance matched traces of equal lengths. Insert tuning peaking inductors and capacitors on both the HVD_ and D_ pins to tune out parasitic capacitance. The values are layout dependent. Contact Maxim Applications for assistance.

±15kV ESD Protection

Maxim devices incorporate structures to protect against electrostatic discharges that may be encountered during handling and assembly.Maxim's state-of-the-art structures protect against ESD of ±15kV on HVD+, HVD-, and HVBUS. The ESD structures withstand high ESD in all states: normal operation, shutdown, and power-down. While other solutions can latch up and require cycling power to resume operation after an ESD event, this device continues to work without latchup. The devices are characterized for protection to the following limits:

1) ±15kV using the Human Body Model
2) ±15kV using the IEC 61000-4-2 Air-Gap method
3) ±8kV using the IEC 61000-4-2 Contact Discharge method

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 9 shows the Human Body Model, and Figure 10 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The devices help users design equipment that meets Level 4 of IEC 61000-4-2.

The Human Body Model testing is performed on unpowered devices, while IEC 61000-4-2 is performed while the device is powered. The main difference between tests done using the Human Body Model and tests done using IEC 61000- 4-2 is higher peak current in IEC 61000-4-2 tests. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 11), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 12 shows the current waveform for the ±8kV, IEC 61000-4-2 Level 4, ESD Contact Discharge test. The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method requires connecting the probe to the device before the probe is energized.

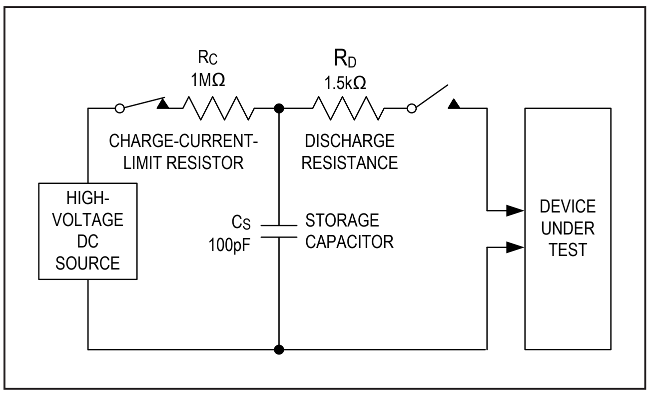


Figure 9. Human Body Test Model

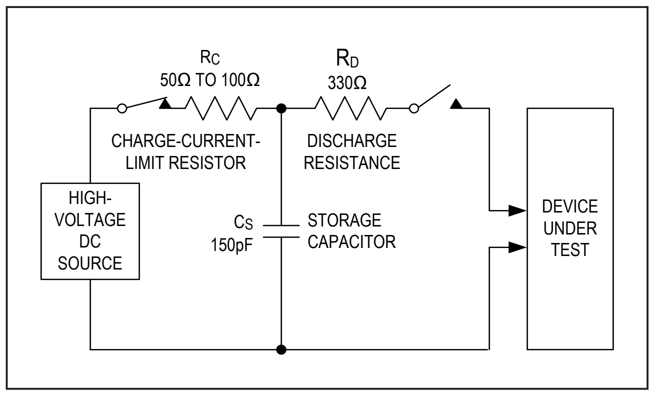


Figure 11. IEC 61000-4-2 ESD Test Model

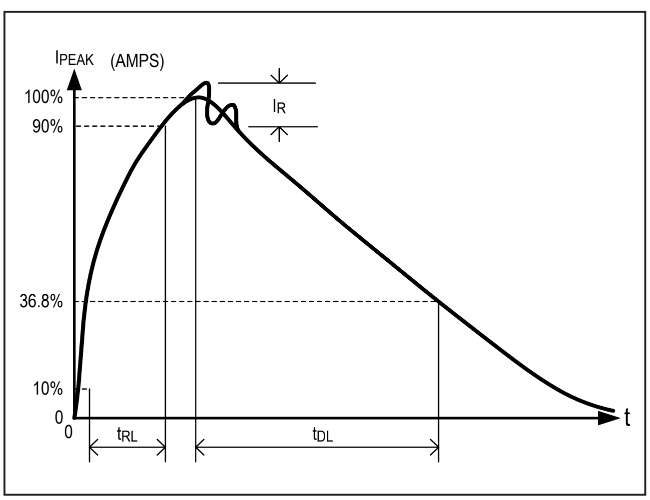


Figure 10. Human Body Current Waveform

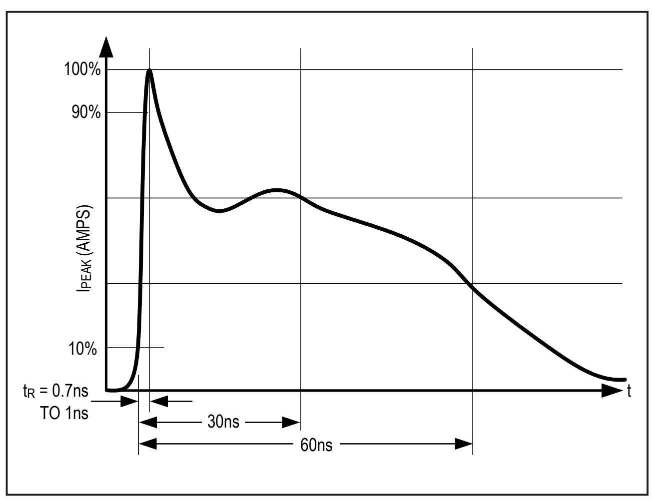
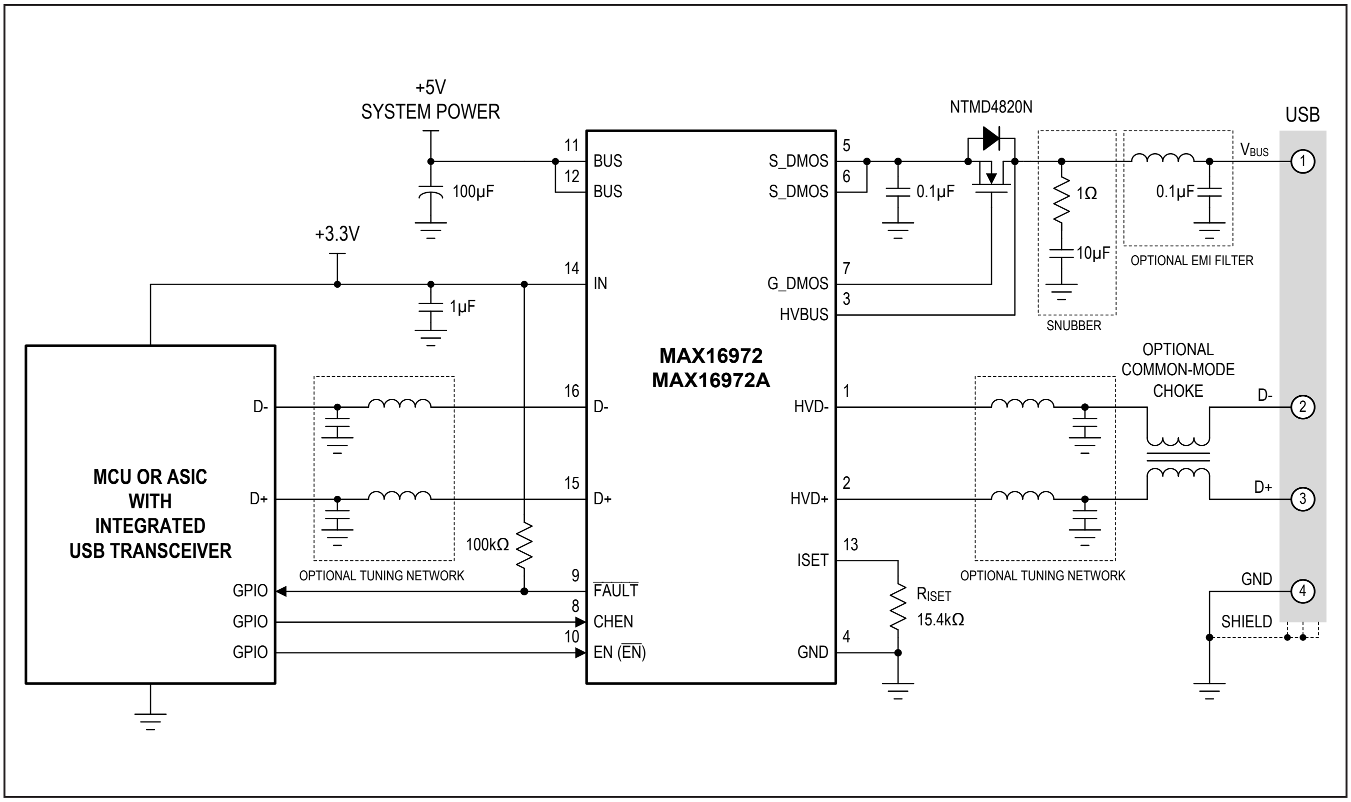


Figure 12. IEC 61000-4-2 ESD Generator Current Waveform

Typical Operating Circuit



Ordering Information

PART	PIN-PACKAGE	ENABLE POLARITY	USB MODES SUPPORTED
MAX16972GTEA/V+	16 TQFN-EP*	Low	1A/DCP
MAX16972GEEA/V+	16 QSOP	Low	1A/DCP
MAX16972GEEB/V+	16 QSOP	Low	1A/2.1A/DCP, OTG
MAX16972GTEB/V+	16 TQFN-EP*	Low	1A/2.1A/DCP, OTG
MAX16972AGTEA/V+	16 TQFN-EP*	High	1A/DCP
MAX16972AGEEA/V+	16 QSOP	High	1A/DCP
MAX16972AGTEB/V+	16 TQFN-EP*	High	1A/2.1A/DCP, OTG
MAX16972AGEEB/V+	16 QSOP	High	1A/2.1A/DCP, OTG

Notes: *All devices operate over the -40°C to +105°C temperature range and support USB CDP/HS modes.*

To order tape and reel, add a T at the end of the part (e.g., MAX16972GEEB/V+T).

/V Denotes an automotive-qualified part.

+ Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/18	Initial release	—
1	8/18	Corrected various typos and made updates to the *Electrical Characteristics* table, Figure 5, Figure 6, Figure 7, TOC 19, TOC 24, TOC 25, *Pin Description*, *Power-Supply Bypass Capacitor* section, *Typical Operating Circuit*, and *Ordering Information*	4, 12, 13, 17, 18, 25, 27, 28

