Low Distortion, 3.2 GHz, RF DGA

Data Sheet **ADA4961**

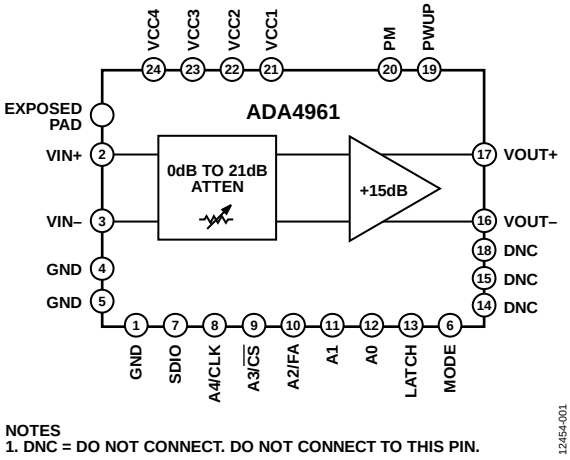
FEATURES

- **High speed**
  - **−3 dB bandwidth: 3.2 GHz**
  - **−1 dB bandwidth: 1.8 GHz**
  - **Slew rate: 12,000 V/µs**
- **Digitally adjustable gain**
  - **Voltage gain: −6 dB to +15 dB**
  - **Power gain: −3 dB to +18 dB**
  - **5-bit parallel or SPI bus gain control with fast attack**
- **IMD3/HD3 distortion, maximum gain, 5 V, high performance (HP) mode**
  - **IMD3/HD3 at 1 GHz: −90 dBc/−83 dBc**
  - **IMD3/HD3 at 1.5 GHz: −85 dBc/−75 dBc**
  - **IMD3/HD3 at 2 GHz: −70 dBc/−70 dBc**
- **Low noise**
  - **Noise density referred to output (RTO): −154 dBm/Hz**
  - **Noise figure: 5.5 dB at A_V = 15 dB, 1 GHz**
- **Differential impedances: 100 Ω input, 50 Ω output**
- **Low power mode operation, power-down control**
- **Single 3.3 V or 5 V supply operation**
- **Available in 24-lead, 4 mm × 4 mm LFCSP**

APPLICATIONS

- **ADC driver for 10-bit to 14-bit GSPS converters**
- **RF/IF gain blocks**
- **Line drivers**
- **Instrumentation**
- **Satellite communications**
- **Data acquisition**
- **Military systems**

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 1.

GENERAL DESCRIPTION

The ADA4961 is a high performance, BiCMOS RF digital gain amplifier (DGA), optimized for driving heavy loads out to 2.0 GHz and beyond. The device typically achieves −90 dBc IMD3 performance at 500 MHz and −85 dBc at 1.5 GHz. This RF performance allows GHz converters to achieve their optimum performance with minimal limitations of the driver amplifier or constraints on overall power that typically result from GaAs amplifiers. This device can easily drive 10-bit to16-bit HS converters.

For many receiver applications, antialias filter (AAF) designs can be simplified or not required.

The ADA4961 has an internal differential input impedance of 100 Ω and a differential dynamic output impedance of 50 Ω, eliminating the need for external termination resistors. The digital adjustability provides for 1 dB resolution, thus optimizing the signal-to-noise ratio (SNR) for input levels spanning 21 dB.

The ADA4961 is optimized for wideband, low distortion performance at frequencies up to 2 GHz. These attributes, together with wide gain adjustment and relatively low power, make the ADA4961 the amplifier of choice for many high speed applications, including IF, RF, and broadband applications where dynamic range at very high frequencies is critical.

The ADA4961 is ideally suited for driving not only analog-to-digital converters (ADCs), but also mixers, pin diode attenuators, SAW filters, and multielement discrete devices. It is available in a 4 mm × 4 mm, 24-lead LFCSP and operates over a temperature range of −40°C to +85°C.

Rev. C **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support **www.analog.com**

TABLE OF CONTENTS

REVISION HISTORY

7/2019—Rev. B to Rev. C

Replaced Figure 11 ... 9

3/2019—Rev. A to Rev. B

Changes to Figure 45 ... 20
Updated Outline Dimension ... 24
Changes to Ordering Guide ... 24

12/2014—Rev. 0 to Rev. A

Changes to Features Section ... 1
Changes to Table 2 ... 4
Changes to Pin 13, Table 6 ... 7
Added Figure 33; Renumbered Sequentially ... 12
Added Figure 34 and Figure 35 ... 13
Changes to Table 10 ... 17
Changes to Figure 52 ... 23

10/2014—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, HP mode, R_S = 100 Ω differential, R_L = 50 Ω differential, T_A = 25°C, f = 500 MHz, V_O = 1.2 V p-p (or 0.6 V p-p per tone for two-tone IMD3), unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O indicates small signal		3200		MHz
−1 dB Bandwidth	V_O indicates small signal		1800		MHz
Slew Rate	V_O = 2 V step		12000		V/µs
Settling Time to 1.0%	V_O = 2 V step		0.6		ns
Overdrive Recovery Time			1.2		ns
Input Return Loss (S_{11})	500 MHz		−40		dB
Output Return Loss (S_{22})	500 MHz		−30		dB
GAIN					
Voltage Gain	Maximum voltage gain		15		dB
	Minimum voltage gain		−6		
Power Gain	Maximum power gain		18		dB
	Minimum power gain		−3		
Gain Step Size			1.0		dB
Gain Step Error			±0.2		dB
INPUT STAGE					
Input Common-Mode Voltage			1.0		V
Input Resistance	Differential		100		Ω
Maximum AC-Coupled Input Level	Differential		6		V p-p
Input Capacitance	Single-ended		1.3		pF
Common-Mode Rejection Ratio (CMRR)			55		dB
OUTPUT STAGE					
Maximum Output Voltage Swing	V_S = 5.0 V		5.0		V p-p
	V_S = 3.3 V		3.0		V p-p
Differential Output Resistance			50		Ω
DIGITAL LOGIC SPECIFICATIONS					
Input Voltage High, $\overline{CS}$[1], CLK[1], SDIO (V_{IH})		1.4		3.3	V
Input Voltage High, PM (V_{IH})		2.8		3.3	V
Input Voltage Low, $\overline{CS}$[1], CLK[1], SDIO, PM (V_{IL})		0		0.8	V
Output Voltage High, $\overline{CS}$[1], CLK[1], SDIO (V_{OH})	I_{OH} = −100 µA	1.4		3.3	V
Output Voltage Low, $\overline{CS}$[1], CLK[1], SDIO (V_{OL})	I_{OL} = +100 µA	0		0.8	V
POWER SUPPLY					
Operating Range			3.3 to 5.0		V
Quiescent Current	5.0 V, HP mode		154		mA
	5.0 V, low power (LP) mode		131		mA
	5.0 V, power-down mode		7.4		mA
	3.3 V, LP mode		126		mA
	3.3 V, power-down mode		7.2		mA

[1] Dual function pin. Table 1 does not contain the full pin name, only the relevant function of the pin. See the Pin Configuration and Function Descriptions section for complete pin names and descriptions.

NOISE/HARMONIC PERFORMANCE

V_S = 5 V, HP mode, R_S = 100 Ω differential, R_L = 50 Ω differential, T_A = 25°C, f = 500 MHz, V_O = 1.2 V p-p (or 0.6 V p-p per tone for two tone IMD3), LC filter connected, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	3.3 V Supply, Low Power Mode Operation[1]			5.0 V Supply, High Performance Mode Operation			Unit
		Min	Typ	Max	Min	Typ	Max	
AC PERFORMANCE, 100 MHz								
Second Harmonic (HD2)	Maximum gain		−75			−81		dBc
	Minimum gain		−76			−80		dBc
Third Harmonic (HD3)	Maximum gain		−85			−88		dBc
	Minimum gain		−88			−88		dBc
Third-Order Intermodulation Distortion (IMD3)	V_{OUT} = 1.2 V p-p composite (2 MHz spacing)							
	Maximum gain		−100			−100		dBc
	Minimum gain		−95			−100		dBc
1 dB Compression Point (OP1dB)	A_V = 15 dB		17.2			18.8		dBm
Noise Figure (NF)	A_V = 15 dB		6.0			5.8		dB
Noise Density Referred to Output (RTO)	A_V = 15 dB		−154			−154		dBm/Hz
AC PERFORMANCE, 500 MHz								
Second Harmonic (HD2)	Maximum gain		−77			−80		dBc
	Minimum gain		−82			−85		dBc
Third Harmonic (HD3)	Maximum gain		−75			−81		dBc
	Minimum gain		−75			−82		dBc
Third-Order Intermodulation Distortion (IMD3)	V_{OUT} = 1.2 V p-p composite (2 MHz spacing)							
	Maximum gain		−90			−90		dBc
	Minimum gain		−95			−90		dBc
1 dB Compression Point (OP1dB)	A_V = 15 dB		17.8			19.3		dBm
Noise Figure (NF)	A_V = 15 dB		5.8			5.6		dB
Noise Density Referred to Output (RTO)	A_V = 15 dB		−154			−154		dBm/Hz
AC PERFORMANCE, 1 GHz								
Second Harmonic (HD2)	Maximum gain		−83			−84		dBc
	Minimum gain		−83			−80		dBc
Third Harmonic (HD3)	Maximum gain		−78			−83		dBc
	Minimum gain		−77			−83		dBc
Third-Order Intermodulation Distortion (IMD3)	V_{OUT} = 1.2 V p-p composite (2 MHz spacing)							
	Maximum gain		−87			−90		dBc
	Minimum gain		−86			−92		dBc
1 dB Compression Point (OP1dB)	A_V = 15 dB		18.1			21.1		dBm
Noise Figure (NF)	A_V = 15 dB		5.6			5.5		dB
Noise Density Referred to Output (RTO)	A_V = 15 dB		−154			−154		dBm/Hz
AC PERFORMANCE, 1.5 GHz								
Second Harmonic (HD2)	Maximum gain		−73			−76		dBc
	Minimum gain		−75			−77		dBc
Third Harmonic (HD3)	Maximum gain		−75			−75		dBc
	Minimum gain		−75			−75		dBc

Parameter	Test Conditions/Comments	3.3 V Supply, Low Power Mode Operation[1] Min	Typ	Max	5.0 V Supply, High Performance Mode Operation Min	Typ	Max	Unit
Third-Order Intermodulation Distortion (IMD3)	V_{OUT} = 1.2 V p-p composite (2 MHz spacing)							
	Maximum gain		−79			−85		dBc
	Minimum gain		−77			−84		dBc
1 dB Compression Point (OP1dB)	A_V = 15 dB		16.4			18.8		dBm
Noise Figure (NF)	A_V = 15 dB		6.0			6.3		dB
Noise Density Referred to Output (RTO)	A_V = 15 dB		−153			−153		dBm/Hz
AC PERFORMANCE, 2 GHz								
Second Harmonic (HD2)	Maximum gain		−73			−75		dBc
	Minimum gain		−76			−77		dBc
Third Harmonic (HD3)	Maximum gain		−65			−70		dBc
	Minimum gain		−66			−69		dBc
Third-Order Intermodulation Distortion (IMD3)	V_{OUT} = 1.2 V p-p composite (2 MHz spacing)							
	Maximum gain		−64			−70		dBc
	Minimum gain		−65			−70		dBc
1 dB Compression Point (OP1dB)	A_V = 15 dB		14.5			17.0		dBm
Noise Figure (NF)	A_V = 15 dB		8.8			9.0		dB
Noise Density Referred to Output (RTO)	A_V = 15 dB		−150			−150		dBm/Hz

[1] 3.3 V high performance mode is not recommended because IMD performance degrades at hot temperatures.

TIMING SPECIFICATIONS

Table 3.

Parameter	Description	Min	Typ	Max	Unit
t_{CLK}	Serial Clock Period	50			ns
t_{DS}	Setup Time Between Data and Rising Edge of SCLK	5			ns
t_{DH}	Hold Time Between Data and Rising Edge of SCLK	5			ns
t_S	Setup Time Between Falling Edge of $\overline{CS}$ and SCLK				ns
t_H	Hold Time Between Rising Edge of $\overline{CS}$ and SCLK				ns
t_{HIGH}	Minimum Period SCLK Can Be in Logic High State		25		ns
t_{LOW}	Minimum Period SCLK Can Be in Logic Low State		25		ns
t_{ACCESS}	Maximum Time Delay Between Falling Edge of SCLK and Output Data Valid for a Read Operation				ns
t_Z	Maximum Time Delay Between $\overline{CS}$ Deactivation and SDIO Bus Return to High Impedance				ns

Timing Diagram

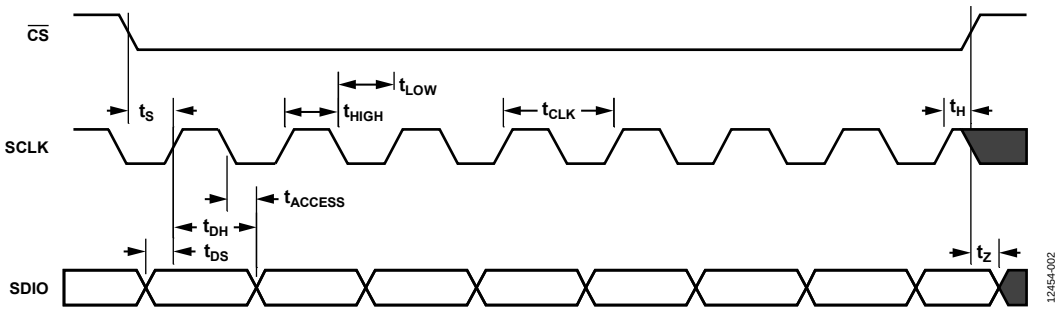


Figure 2.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage, VCCx	5.5 V
PWUP, A4/CLK, A3/$\overline{CS}$, A2/FA, A1, and A0	3.6 V
Input Voltage, VIN+ and VIN−	+3.6 V to −1.2 V
θ_{JA}, Exposed Pad Soldered Down	50.92°C/W
θ_{JC} at Exposed Pad	42.24°C/W
Maximum Junction Temperature	140°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	240°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
24-Lead LFCSP	50.92	42.24	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

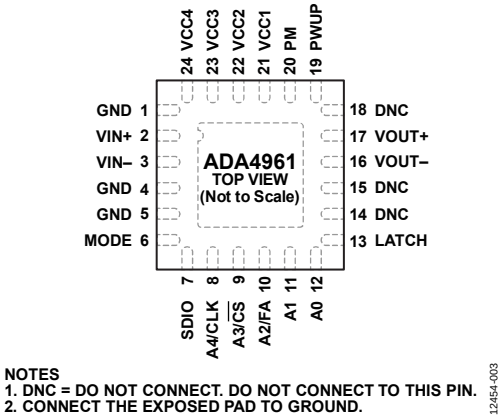


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 5	GND	Power Supply Ground. Connect to system ground plane.
2, 3	VIN+, VIN–	Differential Inputs.
6	MODE	Mode Select Pin for Gain Control. Low indicates serial peripheral interface (SPI), and high (up to 3.3 V) indicates parallel interface.
7	SDIO	Serial Data Input/Output Pin for SPI Gain Control.
8	A4/CLK	Bit A4 for Parallel Gain Control/Serial Clock Pin for SPI Gain Control.
9	A3/$\overline{CS}$	Bit A3 for Parallel Gain Control/Chip Select Pin for SPI Gain Control.
10	A2/FA	Bit A2 for Parallel Gain Control/Fast Attack Pin for SPI Gain Control.
11	A1	Bit A1 for Parallel Gain Control.
12	A0	Bit A0 for Parallel Gain Control.
13	LATCH	Latch Input Asserts Parallel Gain Control. Logic 0 asserts transparent mode, and Logic 1 asserts latched mode.
14, 15, 18	DNC	Do Not Connect. Do not connect to this pin.
16, 17	VOUT–, VOUT+	Differential Outputs.
19	PWUP	Power-Up Control Input Pin. A logic high (3.3 V) asserts power-up. A logic low asserts power-down.
20	PM	Power/Performance Control Input Pin. A logic low indicates high power and high performance, and a logic high indicates low power and nominal performance. Low power mode must be asserted with V_{MIN} = 2.8 V.
21	VCC1	Positive Power Supply. Connect to 5 V or 3.3 V.
22	VCC2	Positive Power Supply. Connect to 5 V or 3.3 V.
23	VCC3	Positive Power Supply. Connect to 5 V or 3.3 V.
24	VCC4	Positive Power Supply. Connect to 5 V or 3.3 V.
	EPAD	Exposed Pad. Connect the exposed pad to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

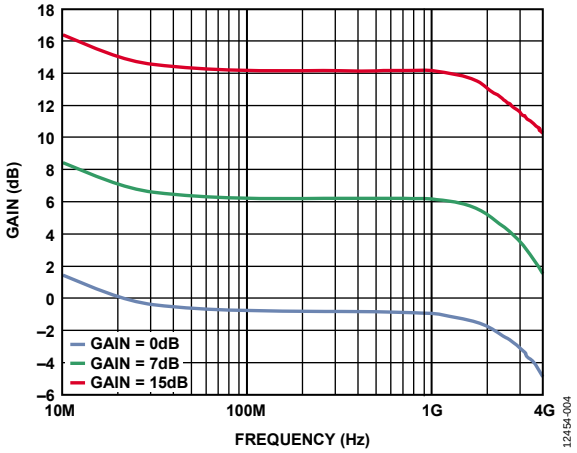


Figure 4. Gain vs. Frequency at 15 dB, 7 dB, and 0 dB Gain Settings, 5.0 V

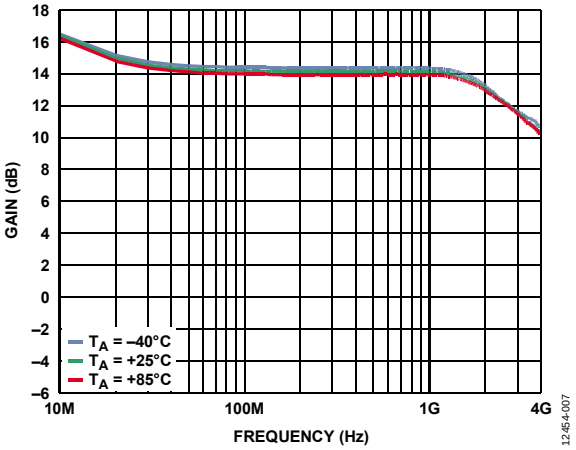


Figure 7. Maximum Gain vs. Frequency at Three Temperatures, 3.3 V, with Low-Pass Filter

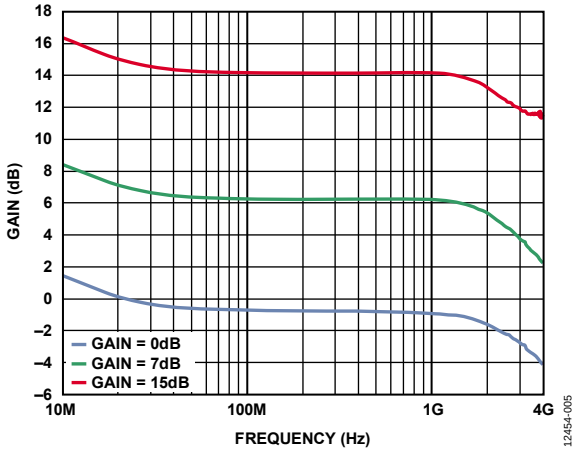


Figure 5. Gain vs. Frequency at 15 dB, 7 dB, and 0 dB Gain Settings, 3.3 V

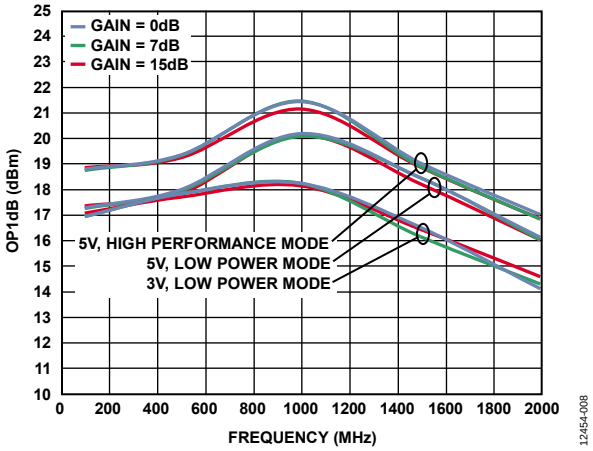


Figure 8. OP1dB vs. Frequency at15 dB, 7 dB, and 0 dB Gain Settings, 5.0 V, 3.3 V, with Low-Pass Filter

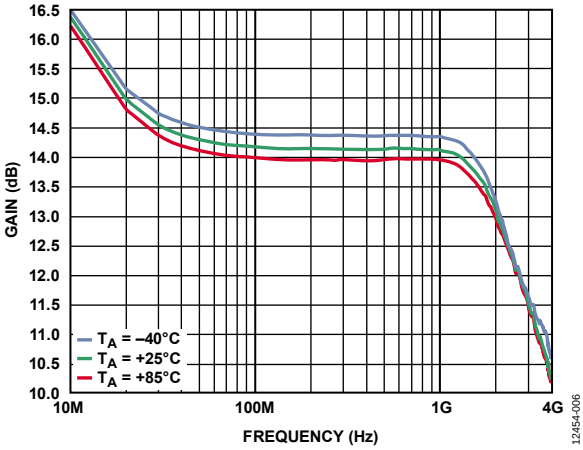


Figure 6. Maximum Gain vs. Frequency at Three Temperatures, 5.0 V, with Low-Pass Filter

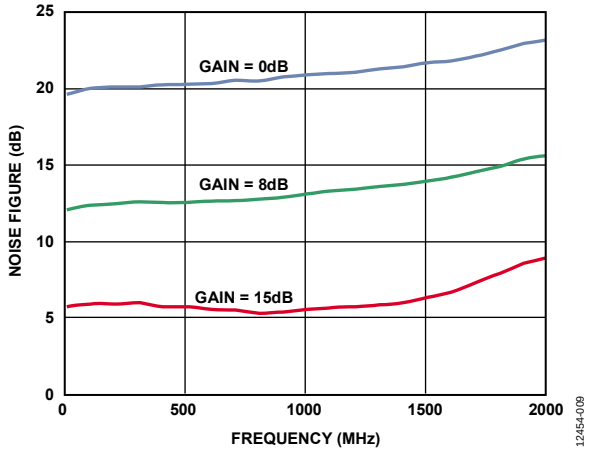


Figure 9. Noise Figure vs. Frequency at 15 dB, 8 dB, and 0 dB Gain Settings, 5.0 V, with Low-Pass Filter

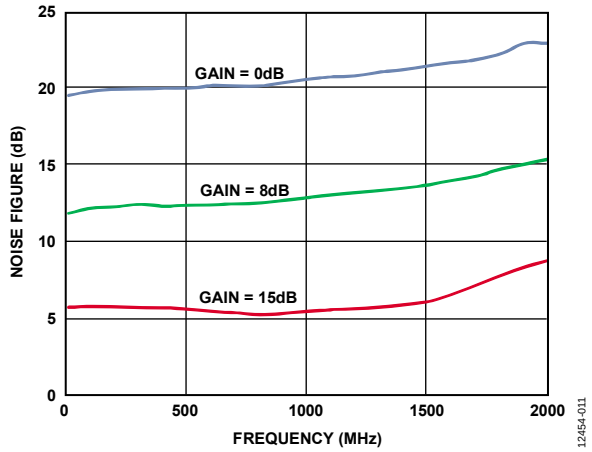


Figure 10. Noise Figure vs. Frequency at 15 dB, 8 dB, and 0 dB Gain Settings, 3.3 V, with Low-Pass Filter

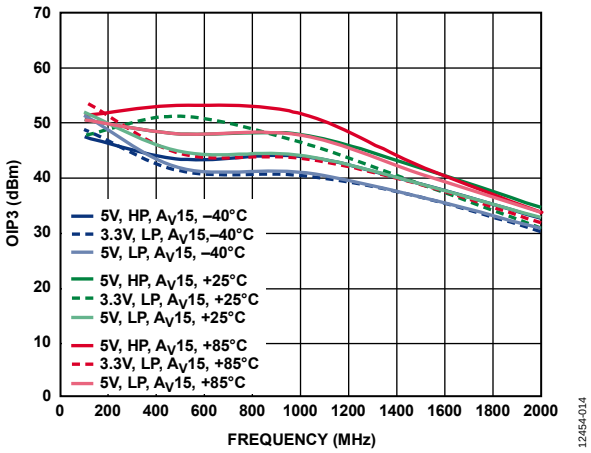


Figure 13. OIP3 vs. Frequency at Three Temperatures, Maximum Gain, 5.0 V, 3.3 V, with Low-Pass Filter

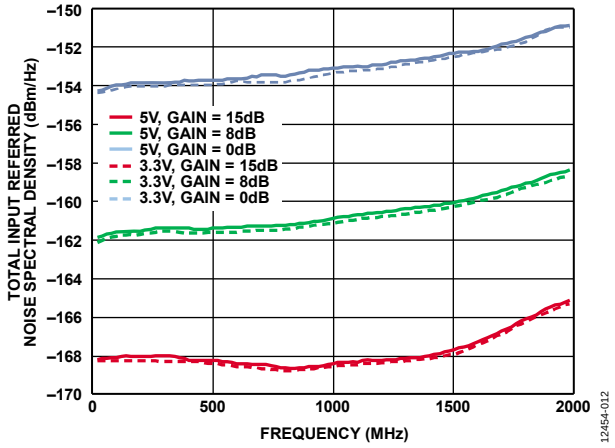


Figure 11. Total Input Referred Noise Spectral Density vs. Frequency at 15 dB, 8 dB, and 0 dB, Gain Settings 5.0 V and 3.3 V, with Low-Pass Filter

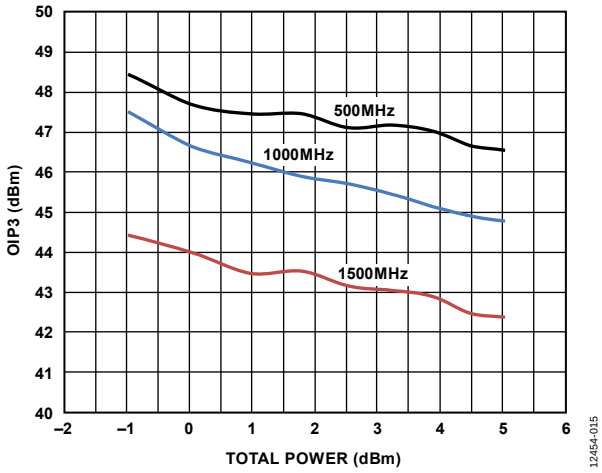


Figure 14. OIP3 vs. Total Power at Three Frequencies

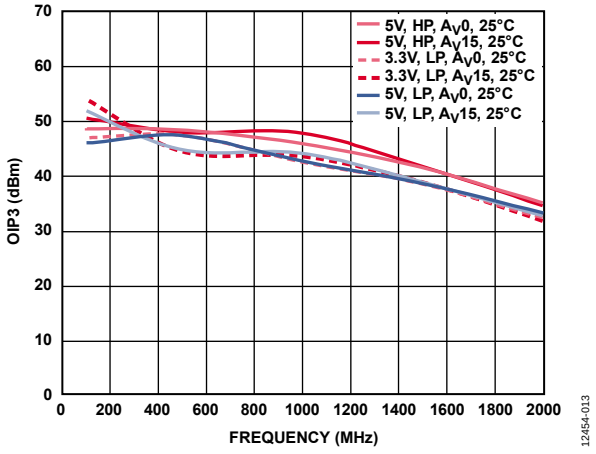


Figure 12. OIP3 vs. Frequency at 15 dB and 0 dB Gain Settings, 5.0 V, 3.3 V, with Low-Pass Filter

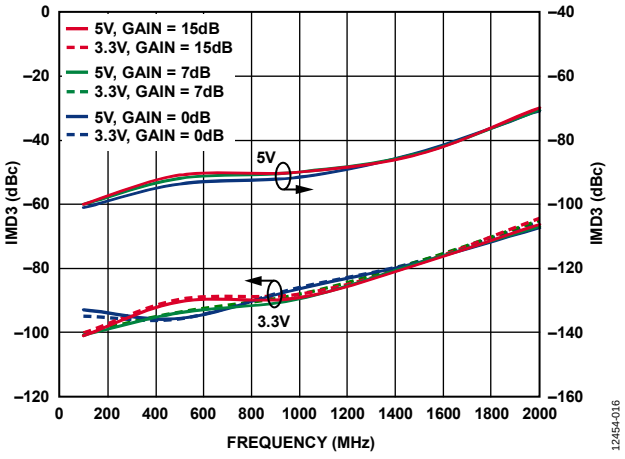


Figure 15. IMD3 vs. Frequency at 15 dB, 7 dB, and 0 dB Gain Settings, 5.0 V, 3.3 V, with Low-Pass Filter,

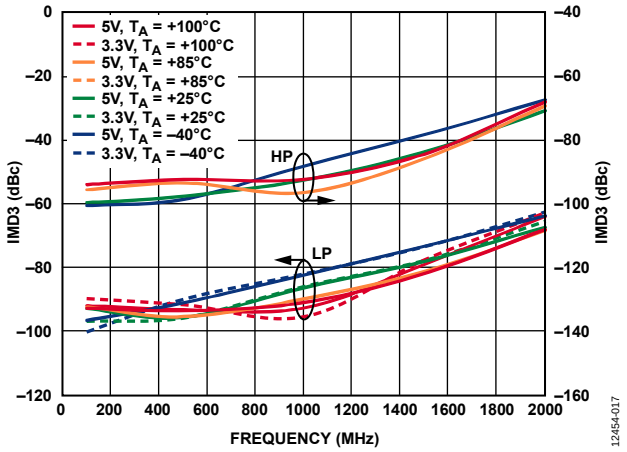


Figure 16. IMD3 vs. Frequency at Maximum Gain, Three Temperatures, 5.0 V, 3.3 V, with Low-Pass Filter

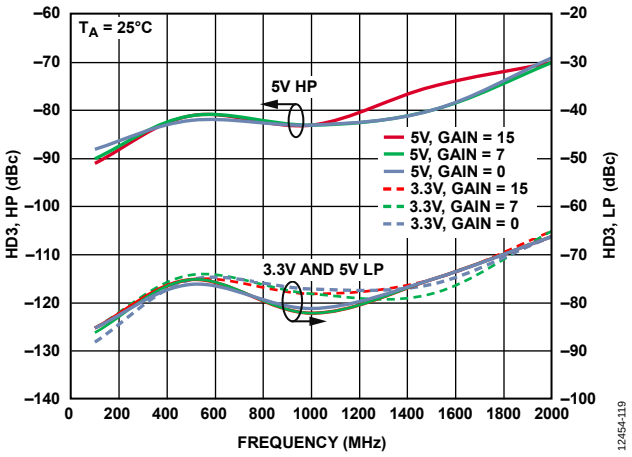


Figure 19. HD3 vs. Frequency at 15 dB, 7 dB, and 0 dB Gain Settings, +5.0 V, +3.3 V, with Low-Pass Filter

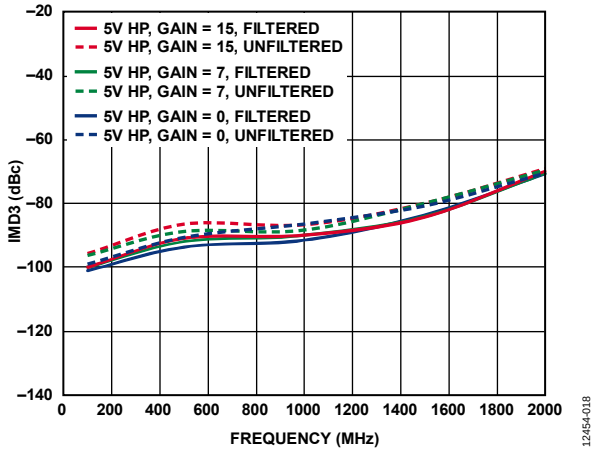


Figure 17. IMD3 vs. Frequency at 15 dB, 7 dB, and 0 dB Gain Settings, with and Without Low-Pass Filter, +5.0 V

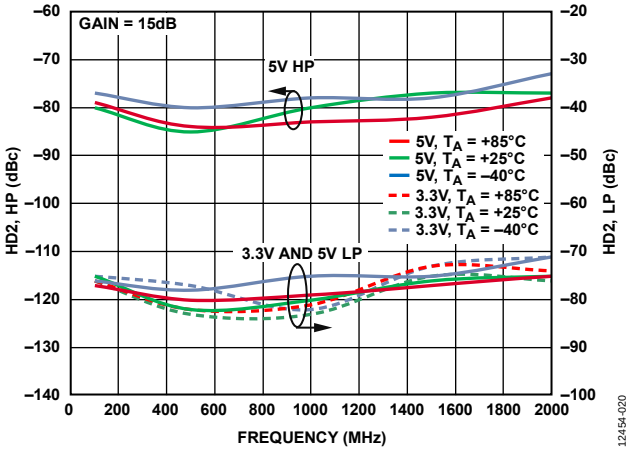


Figure 20. HD2 vs. Frequency at Three Temperatures, +5.0 V, +3.3 V, with Low-Pass Filter

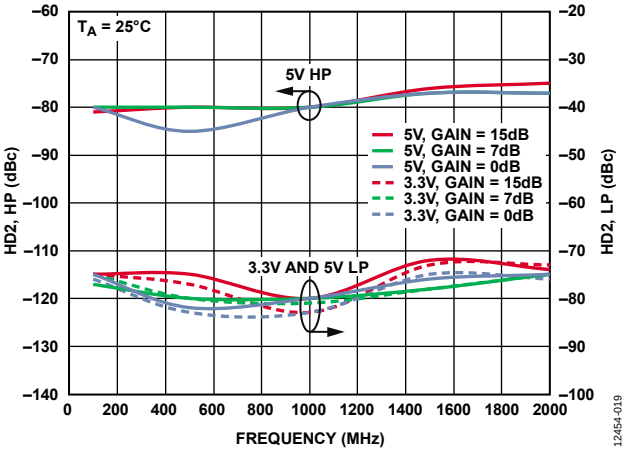


Figure 18. HD2 vs. Frequency at 15 dB, 7 dB, and 0 dB Gain Settings, +5.0 V, +3.3 V, with Low-Pass Filter

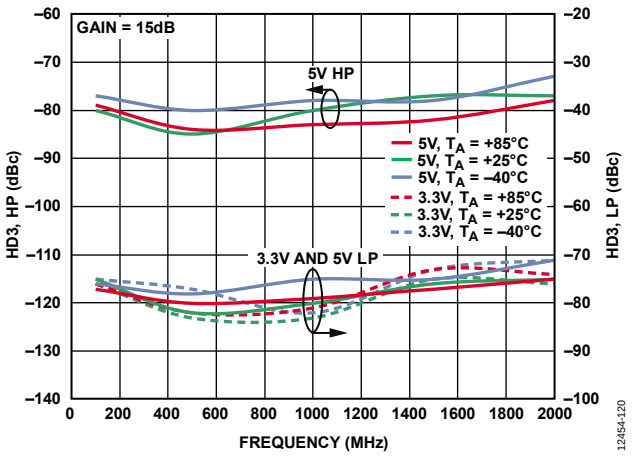


Figure 21. HD3 vs. Frequency at Three Temperatures, 5.0 V, 3.3 V, with Low-Pass Filter

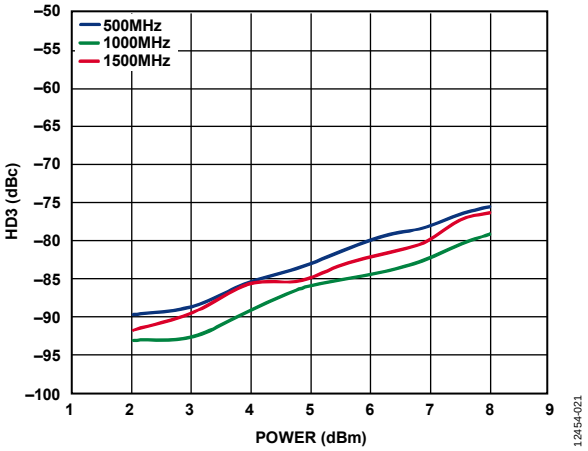


Figure 22. HD3 vs. Output Power/Tone, with Low-Pass Filter

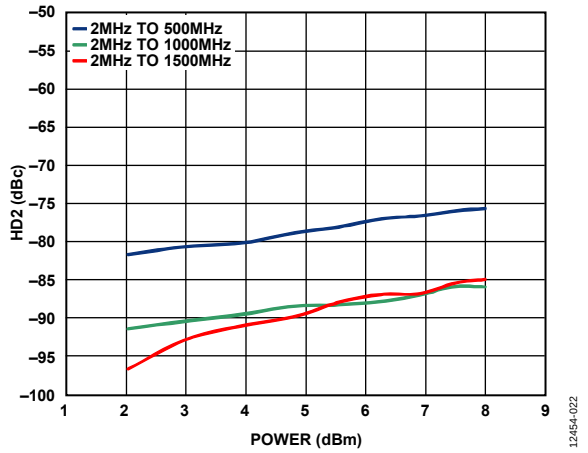


Figure 23. HD2 vs. Output Power/Tone, with Low-Pass Filter

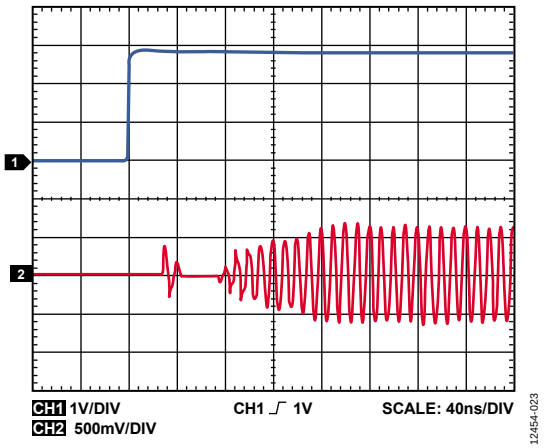


Figure 24. Enable Response Time

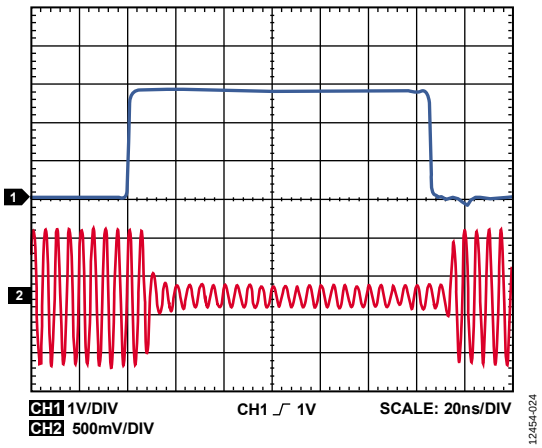


Figure 25. Gain Step Response

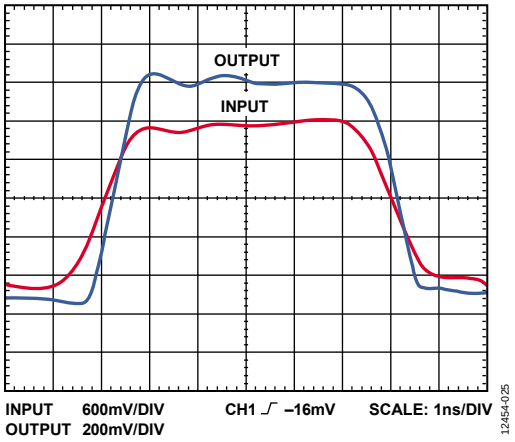


Figure 26. Large Signal Pulse Response

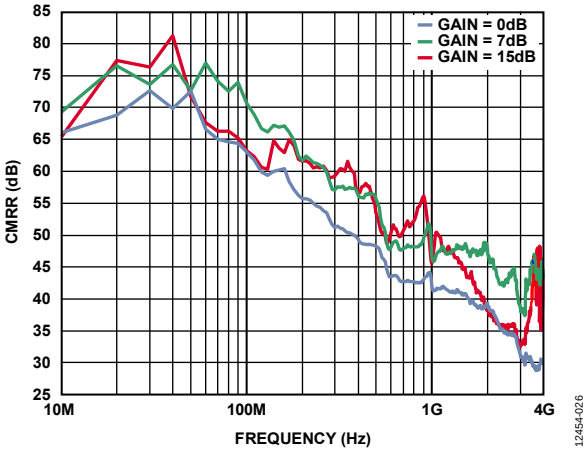


Figure 27. CMRR vs. Frequency at 15 dB, 7 dB, and 0 dB Gain Settings, 5.0 V

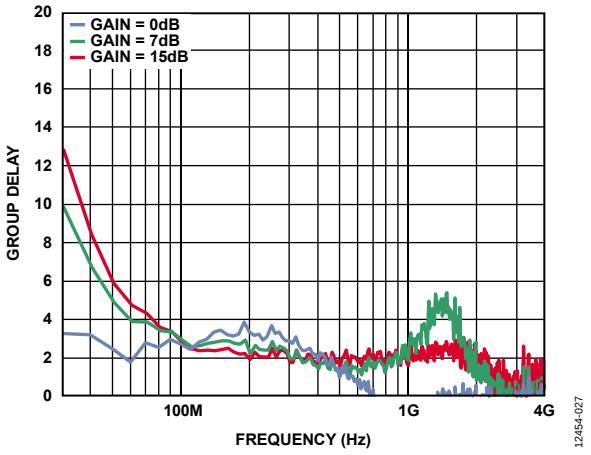


Figure 28. Group Delay vs. Frequency at 15 dB, 7 dB, and 0 dB Gain Settings, 5.0 V

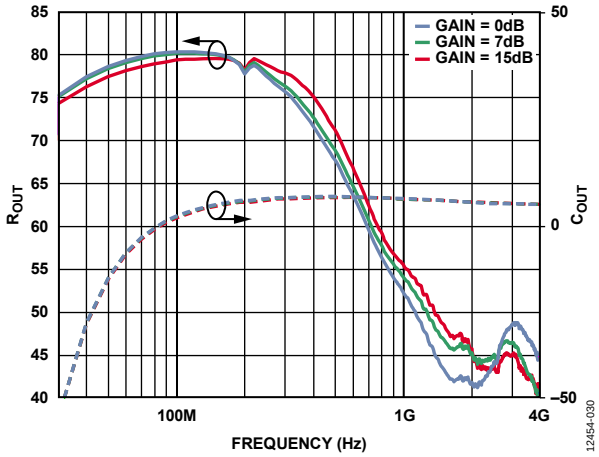


Figure 31. S_{22} RLC vs. Frequency at 15 dB, 7 dB, and 0 dB Gain Settings, 5.0 V

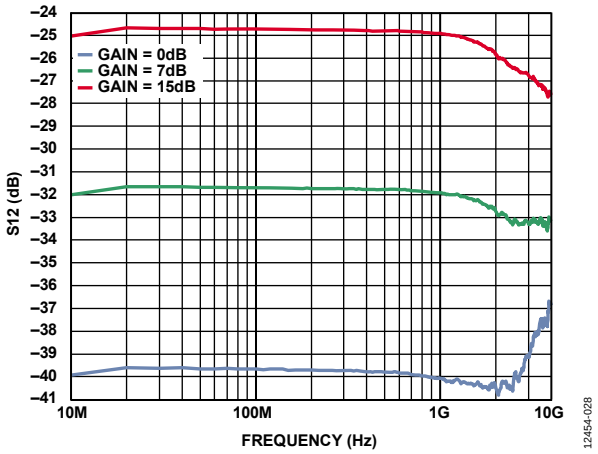


Figure 29. S_{12} vs. Frequency at 15 dB, 7 dB, and 0 dB Gain Settings, 5.0 V

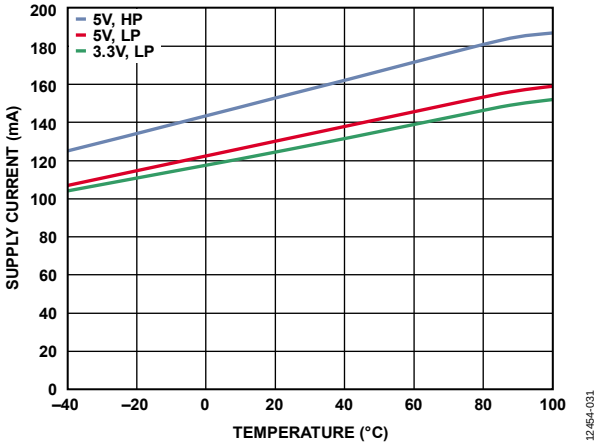


Figure 32. Supply Current vs. Temperature

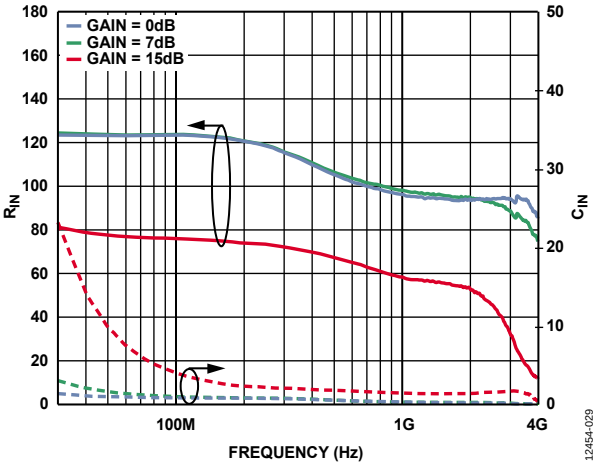


Figure 30. S_{11} Resistor-Inductor-Capacitor (RLC) vs. Frequency at 15 dB, 7 dB, and 0 dB Gain Settings, 5.0 V

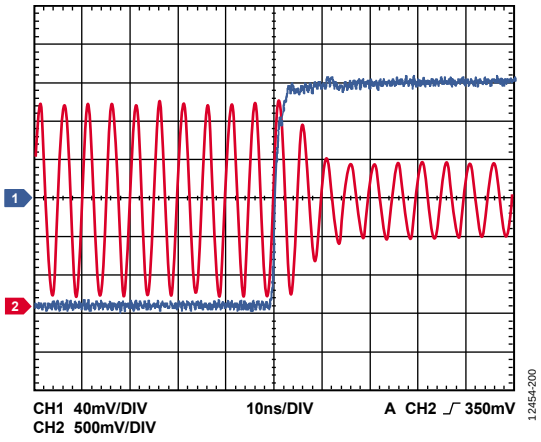


Figure 33. Fast Attack Assertion Time, High Gain to Low Gain, 8 dB Step

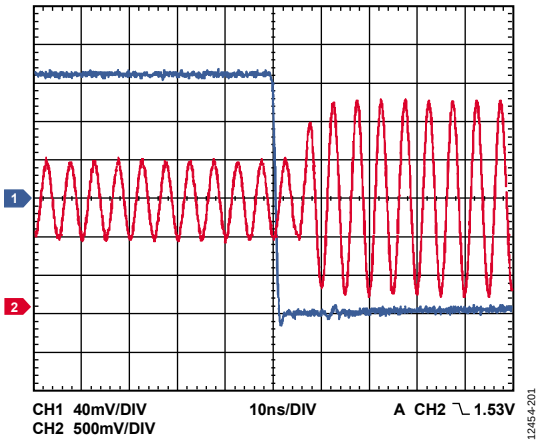


Figure 34. Fast Attack Assertion Time, Low Gain to High Gain, 8 dB Step

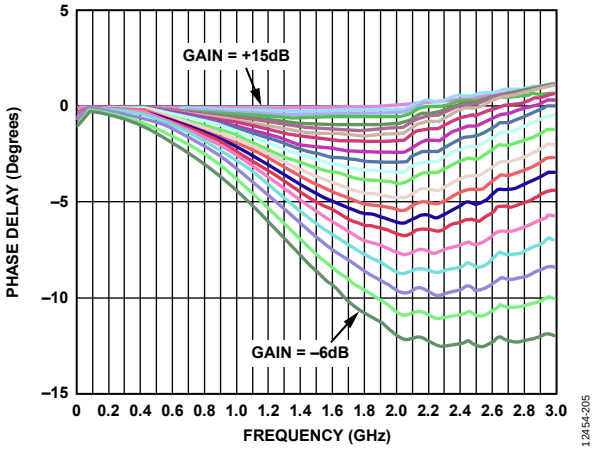


Figure 35. Phase Delay vs. Frequency for all Gain Settings

CHARACTERIZATION AND TEST CIRCUITS

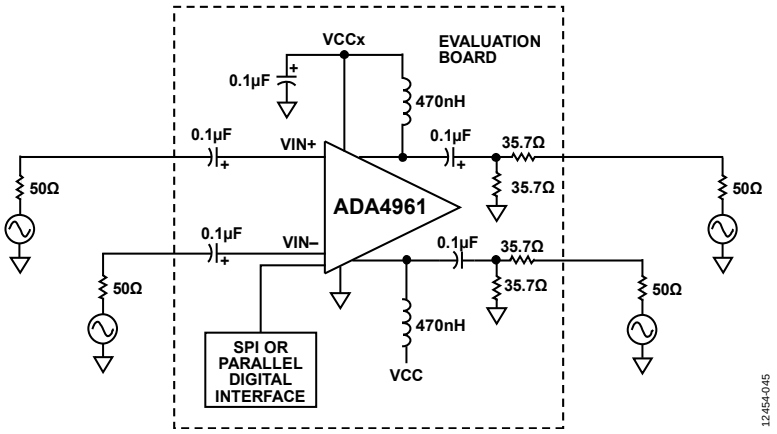


Figure 36. Test Circuit for S-Parameters on Dedicated 50 Ω Differential to Differential Board

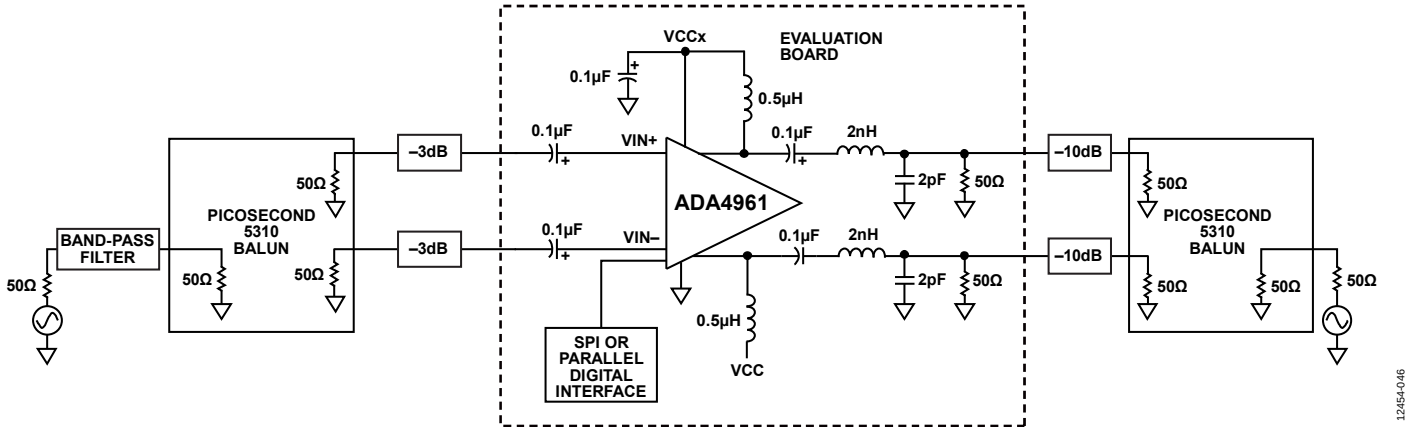


Figure 37. Test Circuit for Single Tone Distortion

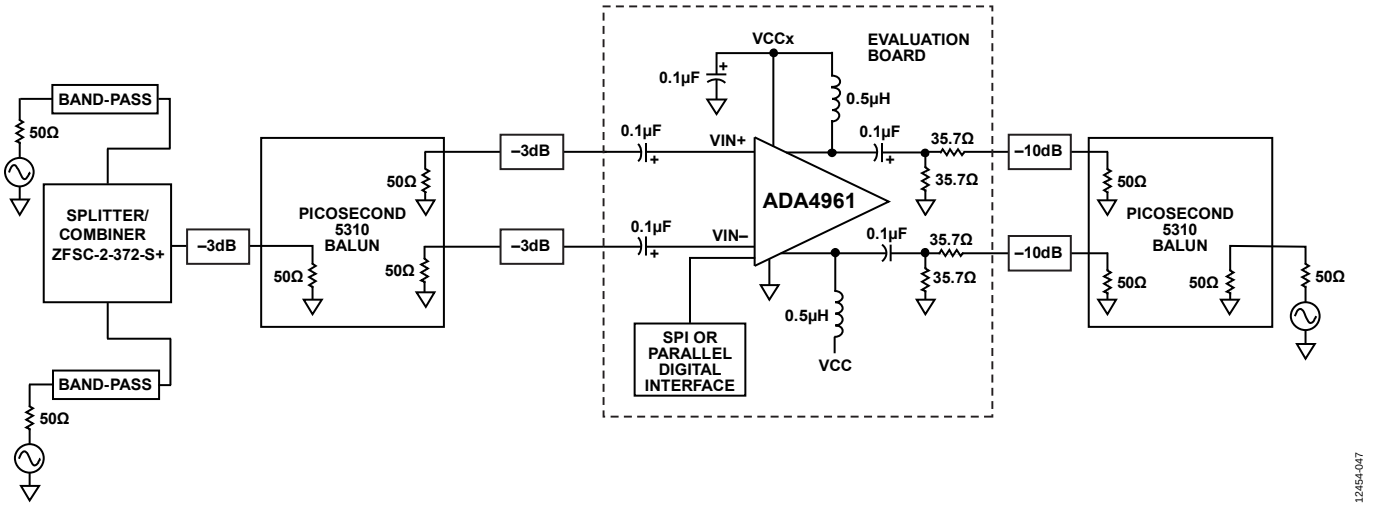


Figure 38. Test Circuit for IMD3/IMD2

AC CHARACTERIZATION OUTPUT FILTER

Figure 37 is used in part of the ac characterization of the ADA4961. The picosecond 5310 balun provides the differential input signal and the 100 Ω differential match to the device. The 3 dB pads make the picosecond balun 50 Ω impedance less reactive on one side, which balances the differential phase accuracy. On the outputs, the 2 nH and 2 pF create a two-pole low-pass filter, along with the two 50 Ω resistors in parallel with the pads and output picosecond balun. This filter creates the 50 Ω differential load.

The output pads make the load more balanced. This is essential for good HD2 performance. This filter technique also creates a lighter load (slight peaking) for the device at higher frequencies, which improves the IMD3 performance. Though the filter bandwidth (BW) computes to 3.3 GHz, the parasitic C (not shown in Figure 37) across the 2 nH filter inductors reduces the 3 dB BW to about 2 GHz (see Figure 4). The filter, beyond reducing integrated output noise, also reduces the higher frequency second and third harmonics above 1 GHz and 700 MHz, respectively (see Figure 20 and Figure 21).

THEORY OF OPERATION

DIGITAL INTERFACE OVERVIEW

The ADA4961 DGA has two digital gain control options: the parallel control interface and the serial peripheral interface. The desired gain control option is selected via the control pin, MODE (see Table 7 for the truth table for the mode control pins). The gain code is in a binary format. A voltage of 1.4 V to 3.3 V is required for a logic high.

Two pins are common to both gain control options: PM and PWUP. PM allows the user to choose operation in low power mode (logic high) or high performance mode (logic low). PWUP is the power-up pin. The physical pins are shared between the two interfaces, resulting in two different functions per digital pin (see Table 2).

Table 7. Digital Control Interface Selection Truth Table

Mode	Interface
1	Parallel control
0	SPI

PARALLEL DIGITAL INTERFACE

The parallel digital interface uses five binary bits (Bits[A4:A0]) and a latch pin. The LATCH pin controls whether the input data latch is transparent or latched. In transparent mode, gain changes as input gain control bits change. In latched mode, gain is determined by the latched gain setting and does not change with changing input gain control bits.

SERIAL PERIPHERAL INTERFACE (SPI)

The SPI uses three pins: SDIO, A4/CLK, and A3/$\overline{CS}$. The SPI data register consists of eight bits, five gain control bits, two fast attack attenuation step size address bits, and one read/write bit. SDIO is the serial data input and output pin. The A4/CLK pin is the serial clock, and A3/$\overline{CS}$ is the channel select pin.

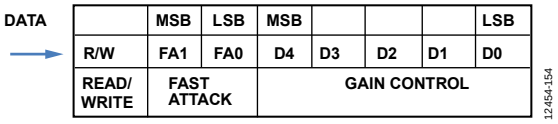


Figure 39. 8-Bit SPI Register

To write to the SPI register, A3/$\overline{CS}$ must be pulled low and eight clock pulses must be applied to A4/CLK. To read the SPI register value, the R/W bit must be set high, A3/$\overline{CS}$ must be pulled low, and the device must be clocked. After the register has been read during the next eight clock cycles, the SPI automatically enters write mode.

Fast Attack

The fast attack feature, accessible via the SPI, allows the gain to reduce from its present setting by a predetermined step size. Four different attenuation step sizes are available. The truth table for fast attack is shown in Table 8.

Table 8. SPI 2-Bit Attenuation Step Size Truth Table

FA1	FA0	Step Size (dB)
0	0	1
0	1	2
1	0	4
1	1	8

SPI fast attack mode is controlled by the A2/FA pin. A logic high on the A2/FA pin results in an attenuation that is selected by Bits[FA1:FA0] in the SPI register.

Table 9. Gain Code vs. Voltage Gain Lookup Table

5-Bit Binary Gain Code	Voltage Gain (dB)
00000	15
00001	14
00010	13
00011	12
00100	11
00101	10
00110	9
00111	8
01000	7
01001	6
01010	5
01011	4
01100	3
01101	2
01110	1
01111	0
10000	−1
10001	−2
10010	−3
10011	−4
10100	−5
10101	−6

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 40 shows the basic connections for operating the ADA4961. Apply a voltage between 3.3 V and 5.0 V to the VCCx pins. Decouple each supply pin with at least one low inductance, surface-mount ceramic capacitor of 0.1 µF, placed as close as possible to the device.

The outputs of the ADA4961 must be pulled up to the positive supply with 0.5 µH RF chokes. The differential outputs are biased to the positive supply and require ac coupling capacitors, preferably 0.1 µF. Similarly, the input pins require ac coupling because they are at bias voltages of about 1 V above ground. The ac coupling capacitors and the RF chokes are the principle limitations for operation at low frequencies.

The digital pins (mode control pins, associated SPI and parallel gain control pins, PM, and PWUP) operate at a voltage of 3.3 V.

To enable the ADA4961, the PWUP pin must be pulled to a logic high. Pulling PWUP low puts the ADA4961 in sleep mode, reducing current consumption to approximately 7 mA at ambient temperature.

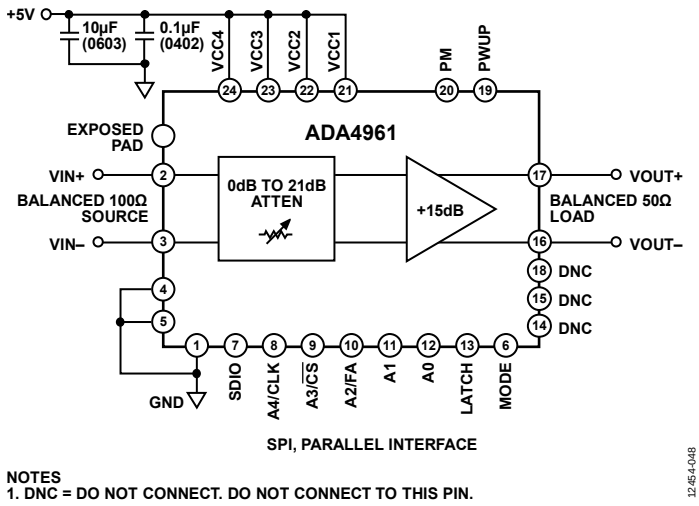


Figure 40. Basic Connections

Table 10. Basic Connections

Pin No.	Mnemonic	Description	Basic Connection
5 V Power			
21	VCC1	Amplifier core power supply	Connect these pins to 5 V and decouple to GND using 10 µF and 0.1 µF capacitors close to the pins.
22	VCC2		
23	VCC3		
24	VCC4		
GND			
1, 4, 5	GND	Ground pins	Connect to ground.
RF Inputs			
2	VIN+	Differential RF inputs, differential input impedance is 100 Ω	Connect these pins to the balanced output of the previous device in the signal chain. A balun can be used to convert from a single-ended signal to differential or to improve even order distortion if the previous device in the signal chain is differential.
3	VIN–		
RF Outputs			
17	VOUT+	Differential RF inputs, differential output impedance is 50 Ω	Connect these pins to the balanced input of the next device in the signal chain. A balun can be used to convert from the ADA4961 differential output to a single-ended signal or to improve even order distortion if the next device in the signal chain is differential.
16	VOUT–		

Pin No.	Mnemonic	Description	Basic Connection
SPI/Parallel Control			
6	MODE	Parallel, serial mode control	Connect this pin to a 3.3 V compliant logic control. Logic 0 asserts serial control, and Logic 1 asserts parallel control.
7	SDIO	SPI data IO	Connect this pin to a 3.3 V compliant logic control.
8	A4/SCLK	SPI clock, parallel mode gain control, Bit 4	Connect this pin to a 3.3 V compliant logic control.
9	A3/$\overline{CS}$	SPI chip select, parallel mode gain control, Bit 3	Connect this pin to a 3.3 V compliant logic control.
10	A2/FA	Fast attack enable, parallel mode gain control, Bit 2	Connect this pin to a 3.3 V compliant logic control. Logic 1 asserts FA enabled, and Logic 0 asserts FA disabled.
11	A1	Parallel mode gain control, Bit 1	Connect this pin to a 3.3 V compliant logic control.
12	A0	Parallel mode gain control, Bit 0	Connect this pin to a 3.3 V compliant logic control.
13	LATCH	Parallel mode latch control	Connect this pin to a 3.3 V compliant logic control. Logic 0 asserts transparent mode, and Logic 1 asserts latched mode.
19	PWUP	Power up	Connect this pin to a 3.3 V compliant logic control. Logic 1 asserts power-up, and Logic 0 asserts power-down.
20	PM	Performance mode	Connect this pin to a 3.3 V compliant logic control. Logic 1 asserts low performance mode, and Logic 0 asserts high performance mode.

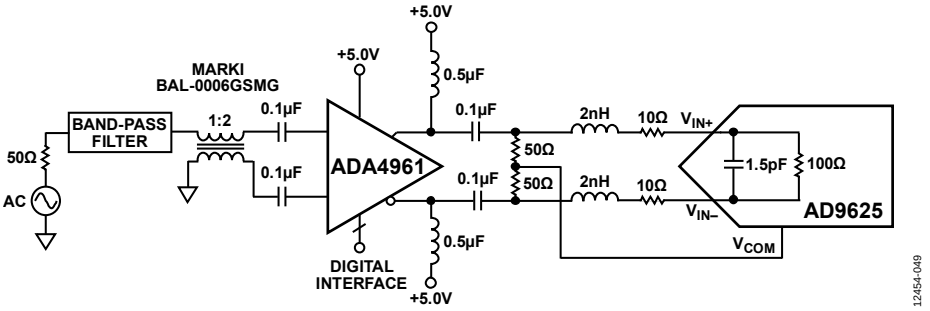


Figure 41. Wideband ADC Interfacing Example Featuring the ADA4961 and the AD9625

ADC DRIVING

The ADA4961 is a high output linearity variable gain amplifier optimized for ADC interfacing. The output IMDs and noise floor remain constant throughout the 22 dB gain range. This is a valuable feature in a variable gain receiver, where it is desirable to maintain a constant, instantaneous dynamic range as the receiver range is modified. The output noise is 6.9 nV/√Hz, which is compatible with 14-bit or 16-bit ADCs. The two-tone IMDs are typically greater than −75 dBc for a 5.5 dBm composite signal into 50 Ω or a 1.2 V p-p composite output. The 50 Ω output impedance makes the task of designing a filter for the high input impedance ADCs more straightforward.

Figure 41 shows the ADA4961 driving a two-pole, 1 GHz, low-pass filter into the AD9625. The AD9625 is a 12-bit, 2.5 GSPS ADC with a buffered wideband input that presents a 100 Ω differential input impedance and requires a 1.2 V input swing to reach full scale. For optimum performance, drive the ADA4961 differentially, using a high performance 1:2 matching balun.

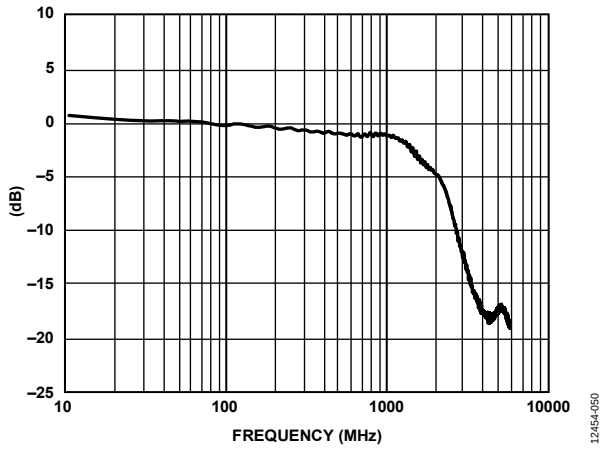


Figure 42. Measured Frequency Response of the Wideband ADC Interface Shown in Figure 41

Figure 41 uses a 1:2 impedance transformer to provide the 100 Ω input impedance of the ADA4961 with a matched input. The open collector outputs of the ADA4961 are biased through the two 0.5 µH inductors, and the two 0.1 µF capacitors on the outputs decouple the 5 V inductor voltage from the input common-mode voltage of the ADA4961. The two 25 Ω resistors, in parallel with the 100 Ω input impedance of the AD9625, provide the 50 Ω load to the ADA4961, where the gain is load dependent. The 2 nH inductors and 1.5 pF internal capacitance of the AD9625 constitute the 1 GHz, 1 dB low-pass filter. The two 5 Ω isolation resistors suppress any switching currents from the ADC input sample-and-hold circuitry. The circuit shown in Figure 41 provides variable gain, isolation, filtering, and source matching for the AD9625. By using this circuit with the ADA4961 in a gain of 15 dB (maximum gain), a full-scale SNR (SNRFS) of 55 dB and an SFDR performance of 77 dBc are achieved at 1 GHz, as shown in Figure 43.

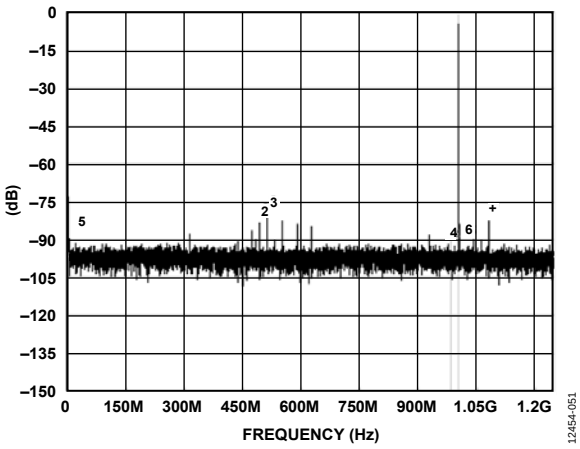


Figure 43. Measured Single Tone Performance of the Circuit Shown in Figure 41 for a 1 GHz Input Signal using Maximum Gain (15 dB)

The two-tone 1 GHz IMDs of two 0.6 V p-p signals have an SFDR of greater than 75 dBc, as shown in Figure 44.

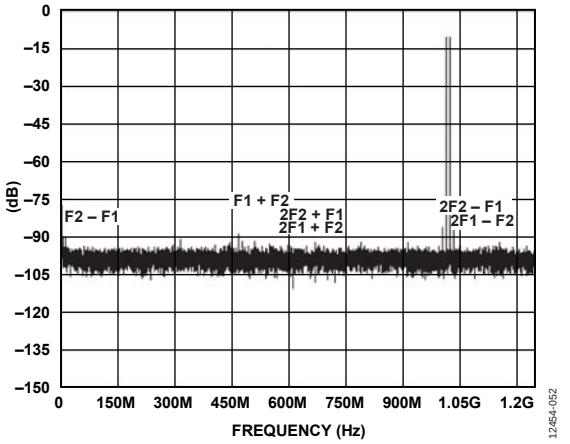


Figure 44. Measured Two-Tone Performance of the Circuit Shown in Figure 41 for a 1 GHz Input Signal Using Maximum Gain (15 dB)

LOW-PASS ANTIALIAS FILTERING FOR THE ADC INTERFACE

The high frequency distortion performance of the ADA4961 can be enhanced by adding a low-pass filter to the output (see Figure 46 and Figure 47. A two-pole low-pass filter is used in the ADC Driving section to illustrate the distortion improvement capabilities and integrated noise reduction. Figure 49 shows a simplified diagram of a two-pole low-pass (LP) filter. The inductor capacitance (LC) values are 2 nH and 2 pF, respectively. This filter gives an overall −3 dB BW of 2 GHz when connected to the ADA4961. Ideally, the BW is 3.5 GHz without any parasitics. The parasitic, C, (about 1 pF) across the 2 nH inductor (not shown) reduces the BW to about 2.1 GHz.

Take care to ensure that the physical length of the filter is less than 1/10 the wavelength of the 3 dB corner frequency. At 2 GHz, it is 75 mm. The Series L (along with the internal bond wire inductance) and C parasitic parallel create a parallel resonance that causes a reduction in overall BW. Other values and filter types can be used depending on the end user requirements, but care is needed to ensure that the Circuit Q does not exceed 1. The values of 2 nH and 2 pF show the relative improvement in distortion (single tone and IMD3) vs. no filter at frequencies out to 1.5 GHz. At frequencies above about 600 MHz, the HD3s begin to attenuate as is expected due to the LP roll-off of the L (2 nH) and Shunt C (2 pF). In addition, the inband IMD3s also improve. This improvement is due to the peaking that results at the amplifier output due to its internal parasitics interacting with the 2 nH inductor and its Shunt C parasitic. This peaking reduces the input signal to the amplifier (not shown), thus reducing inband third-order terms.

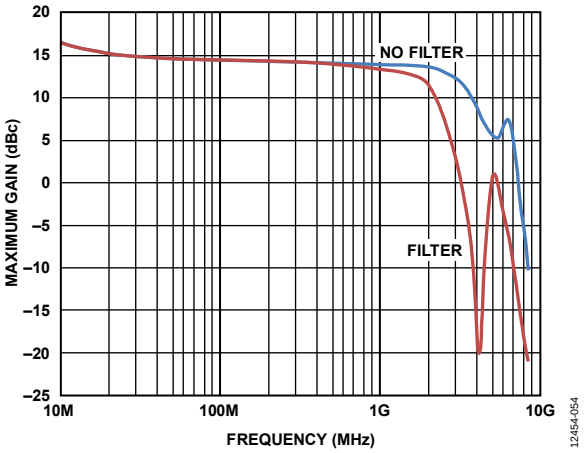


Figure 45. Maximum Gain vs. Frequency, with and Without LC Filter

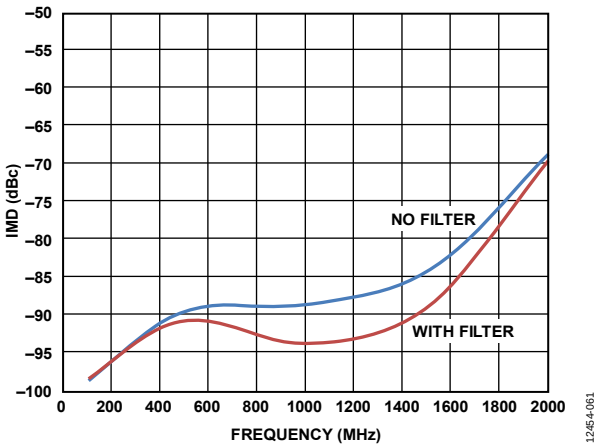


Figure 46. IMD vs. Frequency, with and Without LC Filter

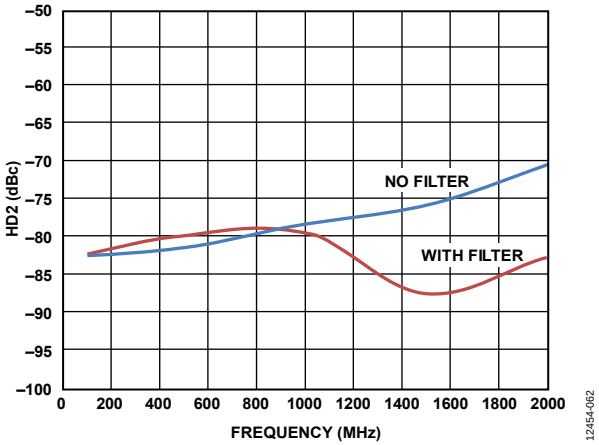


Figure 47. HD2 vs. Frequency, with and Without LC Filter

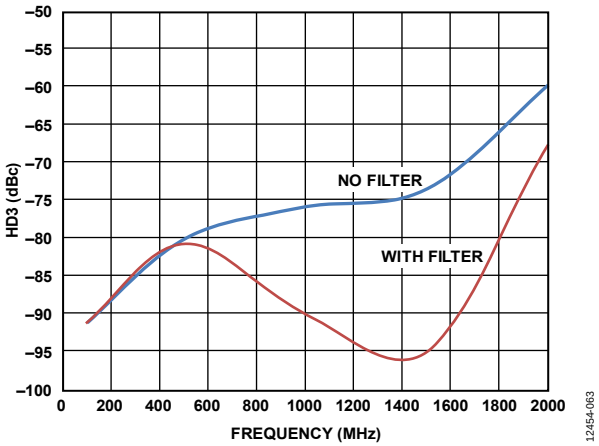


Figure 48. HD3 vs. Frequency, with and Without LC Filter

LAYOUT CONSIDERATIONS

When designing the board, take care to minimize the parasitic capacitance caused by the routing that connects the RF outputs. A good practice is to avoid any ground or power plane under this routing region and under the chokes to minimize the parasitic capacitance.

EVALUATION BOARD

The ADA4961 evaluation board is a 4-layer board built on FR4 material. The board is configured for a single-ended input and a single-ended output. All RF input and output traces are 50 Ω. On the RF input, the Mini-Circuits® TCM2-43X balun, a 2:1 impedance balun, is used to match external 50 Ω generators to the 100 Ω differential input of the ADA4961. On the RF output, the Mini-Circuits TCM1-43X balun, a 1:1 impedance balun, is used to convert the differential output of the amplifier to the single-ended output of the evaluation board.

The outstanding linearity performance over frequency is achieved in part by the RF outputs having a dc bias to the supply, typically 5 V for best performance. RF chokes provide the path to the bias supply from the RF output to the positive supply rail. It is highly recommended that Coilcraft 0805CS-471XJLC 470 nH inductors be used for bias. The self resonant frequency of these inductors is high enough so that it does not impact the performance of the ADA4961 at up to 4 GHz.

A complete description of operating the evaluation board and evaluation board software is given in the EV-ADA4961SDP1Z user guide.

A bill of materials for the RF section of the evaluation board is given in Table 11.

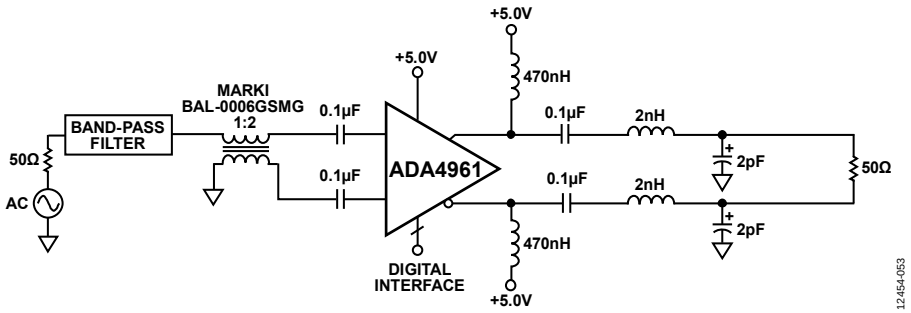


Figure 49. ADC Interface Circuit Using a Low-Pass Antialias Filter

Table 11.

Reference Designator	Description	Manufacturer	Part Number
ADA4961ACPZN-R7	Device under test	Analog Devices, Inc.	ADA4961ACPZN-R7
J1, J2	Input, output SMA connectors	Johnson	142-0701-801
T1	RF input balun	Mini-Circuits	TCM2-43x+
L1, L2	470 nH RF bias chokes	Coilcraft	0805CS-471XJLC
T2	RF output balun	Mini-Circuits	TCM1-43x+
C1, C2, C3, C4	0.1 µF RF dc blocking capacitors	Murata-Erie	GRM155R71C104KA88D
R1, R2	8.87 Ω input matching pad	Panasonic	ERJ2GEJ9R1X

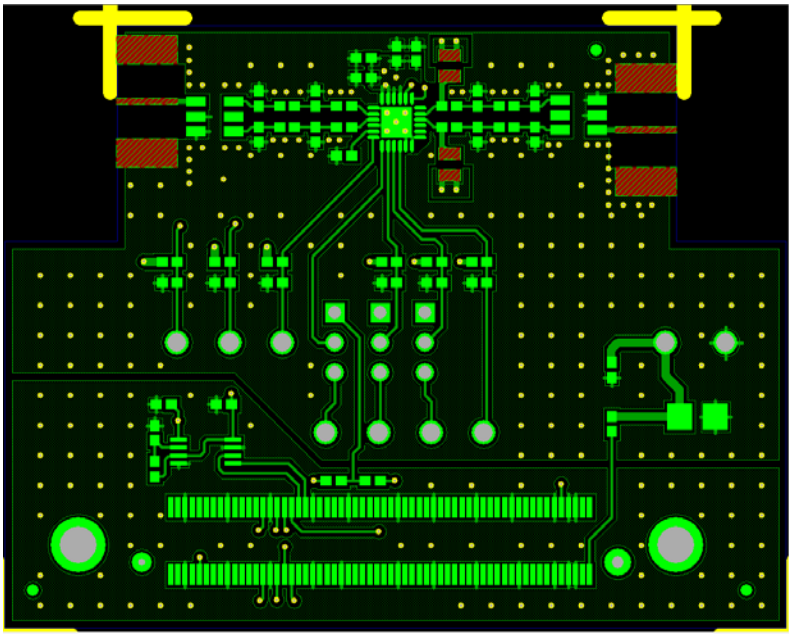


Figure 50. ADA4961 Evaluation Board, Top Layer

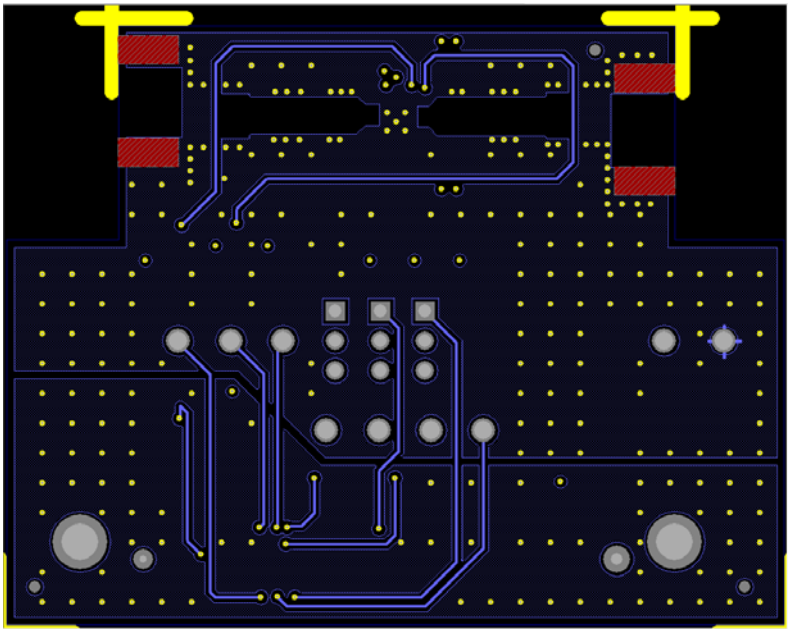


Figure 51. ADA4961 Evaluation Board, Bottom Layer

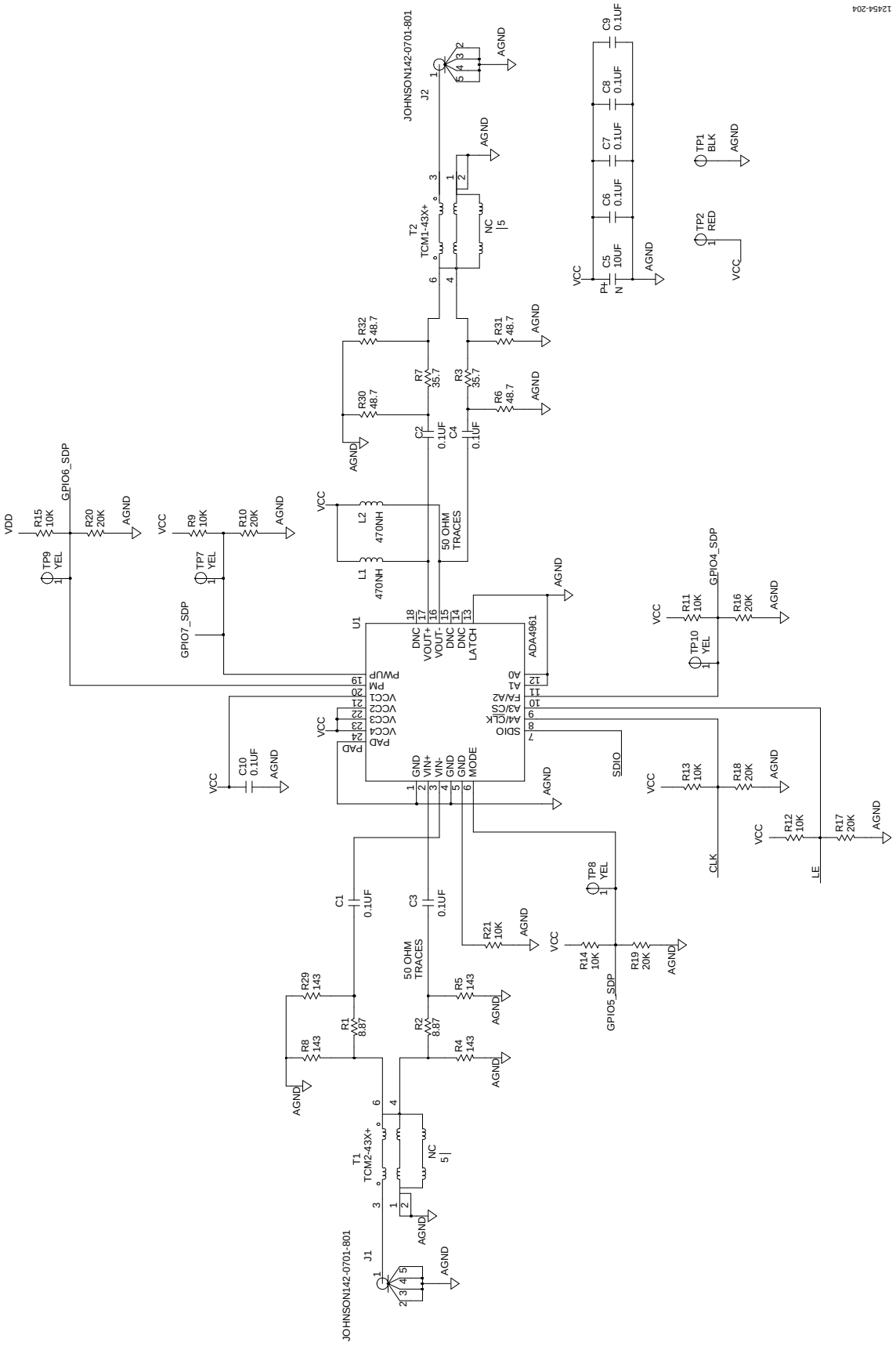


Figure 52. ADA4961 Evaluation Board Schematic

OUTLINE DIMENSIONS

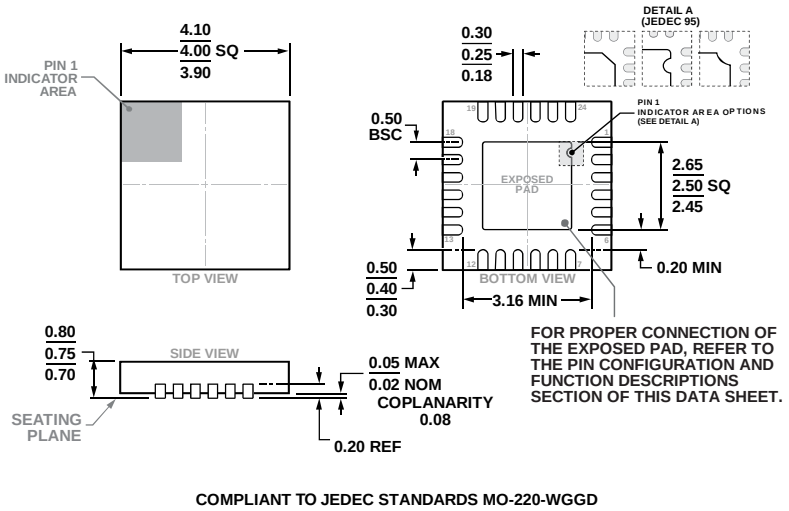


Figure 53. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADA4961ACPZN-R7	−40°C to +85°C	24-Lead LFCSP, 7″ Tape and Reel	CP-24-7
EV-ADA4961SDP1Z	−40°C to +85°C	Evaluation Board	

[1] Z = RoHS Compliant Part.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADA4961ACPZN-R7